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Stress-Strain Management of Heteroepitaxial Polycrystalline Silicon Carbide Films

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Stress-Strain Management of Heteroepitaxial Polycrystalline Silicon Carbide Films

by

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ABSTRACT

Silicon carbide (SiC) is one of the hardest known materials and is also, by good fortune, a wide bandgap semiconductor. While the application of SiC for high-temperature and high-power electronics is fairly well known, its utility as a highly robust, chemically-inert material for microelectrical mechanical systems (MEMS) is only beginning to be well recognized. SiC can be grown on both native SiC substrates or on Si using heteroepitaxial growth methods which affords the possibility to use Si micromachining methods to fabricate advanced SiC MEMS devices.

The control of film stress in heteroepitaxial silicon carbide films grown on polysilicon-on-oxide substrates has been investigated. It is known that the size and structure of grains within polycrystalline films play an important role in determining the magnitude and type of stress present in a film, i.e. tensile or compressive. Silicon carbide grown on LPCVD polysilicon seed-films exhibited a highly-textured grain structure and displayed either a positive or negative stress gradient depending on the initial thickness of the polysilicon seed-layer. In addition a high-quality (111) oriented 3C-SiC on (111)Si heteroepitaxial process has been developed and is reported. SiC MEMS structures, both polycrystalline (i.e., poly-3C-SiC) and monocrystalline (i.e., 3C-SiC) were realized using micromachining methods. These structures were used to extract the stress properties of the films, with a particular focus on separating the gradient and uniform stress components.

CHAPTER 1: SILICON CARBIDE: A MATERIAL FOR MICROELECTROMECHANICAL SYSTEMS (MEMS)

1.1 Introduction

Although silicon is a well-suited material for a wide range of sensor and actuator applications, it is limited for electronic devices at temperatures below 250°C. In addition its mechanical properties begin to degrade at temperatures above 600°C (Mehregany, 1998) which limit its use for high temperature and harsh environment applications. Consequently when silicon-based MEMS technology is used in harsh environments, the expensive and bulky cooling and packaging systems that need to be implemented in order to keep the devices within operating limits are expensive or sometimes prohibitive. As the demand grows to implement cost-saving and space-saving microsensor and microactuator technologies in harsh environments, one must look for other material options that can satisfy the requirement of long-term device survivability and low-production costs. To meet the demands for high-temperature (≥ 350°C) MEMS, there is a need for an electronic material exhibiting a wide bandgap, good mechanical (and chemical) stability, and good thermal stability over a large temperature range. An ideal material platform for harsh-environment MEMS would also exhibit an extensive range of robustness that would withstand a multitude of environments. It would be chemically inert to corrosive attack, it would exhibit outstanding wear resistance, it would

demonstrate radiation-hardness (i.e., rad-hard), and it could be biologically implantable. Although this may appear to be an unrealistic "wish-list", there are material candidates that seem to meet these demanding criteria.

Diamond is one such candidate that is currently being explored. It is the hardest known natural material, scoring a 10 on the Mohs hardness scale. It has the highest thermal conductivity of any known material; five times greater than silver, the second highest thermal conductor. It has a wide band gap and can be doped to exhibit semiconductor properties. It has excellent thermal and mechanical stability, except in high-temperature (≥ 700°C) oxygen environments, in which it readily oxidizes (i.e., surface turns to graphite). This drawback excludes it for use as a material for combustion microsensors. Therefore diamond-based MEMS have found limited use, mostly in low-temperature RF applications and in biomedical applications as a coating for Si-based sensors and devices.

Silicon Carbide (SiC) is another candidate that appears to fulfill the requirements of a MEMS platform material for a multitude of harsh environmental conditions. It has long been recognized as a semiconductor with excellent physical, electrical and chemical characteristics (see Table 1.1). It has excellent mechanical and electrical stability at high temperatures. It is inert to nearly all wet chemistry, and it can only be etched by molten alkaline hydroxides at temperatures ≥600°C. Silicon carbide doesn't melt, but sublimes at temperatures exceeding 1800°C. Silicon carbide demonstrates excellent wear resistance, having a 9.15 wear resistance rating as compared to 10 for diamond. It is the third hardest known material, only diamond and boron nitride exceed it. Silicon carbide can be thermally oxidized to form a passivating SiO_2 layer, although the oxidation rate is

slow when compared to silicon. Surface passivation using a hydrogen-terminated surface has been shown to form flatband conditions for several hours (C. Coletti 2008). 100mm diameter silicon carbide wafers grown from bulk crystals are commercially available from several manufacturers; 150mm wafers with defect densities less than 10 cm^{-2} have been recently reported. Monocrystalline and polycrystalline silicon carbide has been epitaxially grown on silicon substrates up to 150mm in diameter.

Table 1.1 Properties of commonly used SiC polytypes compared with Si and Diamond. (Casady and Johnson 1996) (Harris 1995).

Property	4H-SiC	6H-SiC	3C-SiC	Si	Diamond
Energy bandgap at 300K	3.20	3.00	2.29	1.12	5.45
Intrinsic Carrier Concentration at 300K (cm^{-3})	$5x10^{-9}$	$1.6x10^{-6}$	$1.5x10^{-1}$	$1x10^{10}$	$\sim10^{-27}$
Critical breakdown electric field (MV/cm)	2.2	2.5	2.12	0.25	1-10
Saturated electron drift velocity (x 10^7 cm/s)	2.0	2.0	2.5	1.0	1.5
Electron mobility (cm^2/V-s)	1000	600	800	1450	480
Hole mobility (cm^2/V-s)	115	100	40	470	1600
Thermal Conductivity at 300K (W cm^{-1} K^{-1})	3.7	3.6	3.6	1.49	6-20
Coefficient of Thermal Expansion at 300K (10^{-6} K^{-1})	4.3 $\perp$c 4.7 $\parallel$c	4.3 $\perp$c 4.7 $\parallel$c	3.2	3.0	1.0
Lattice constant (a, c in Å)	a=3.0730 c=10.053	a=3.0806 c=15.1173	a=4.3596	a=5.430	a=3.5668
Elastic coefficient* (GPa) *calculated	C_{44}=600	C_{11}=500 C_{12}=92 C_{44}=168	C_{11}=352 C_{12}=120 C_{44}=233	C_{11}=167 C_{12}=65 C_{44}=80	C_{11}=1079 C_{12}=124 C_{44}=578

1.2 Heteroepitaxial Silicon Carbide

Epitaxy is the growth of a thin layer on a crystal substrate in which the substrate is a template for the growth such that the proper atomic arrangement is achieved. Heteroepitaxy is the growth of an epitaxial layer on a seed crystal of a different crystal type. Cubic SiC, more commonly referred to as 3C-SiC, may be heteroepitaxially grown on Si substrates. Since the growth of single crystal, large-area, bulk 3C-SiC crystals has not been demonstrated, heteroepitaxy is needed to grow 3C-SiC crystals. However, the near 20% lattice mismatch between Si and SiC typically leads to an epitaxial film that is highly defective and therefore not suitable for electronic devices. This is generally because interfacial defects propagate into the 3C-SiC device layer and result in high leakage currents in 3C-SiC/Si devices. Indeed, the issues impeding the growth of high quality, monocrystalline 3C-SiC/Si heteroepitaxial films have proven to be so difficult to overcome that many groups have abandoned 3C-SiC/Si. In this thesis, we aim to use a novel substrate alongside a tailored stoichiometric bilayer structure to mitigate film stresses arising from defects with the goal of developing device-quality 3C-SiC/Si layers.

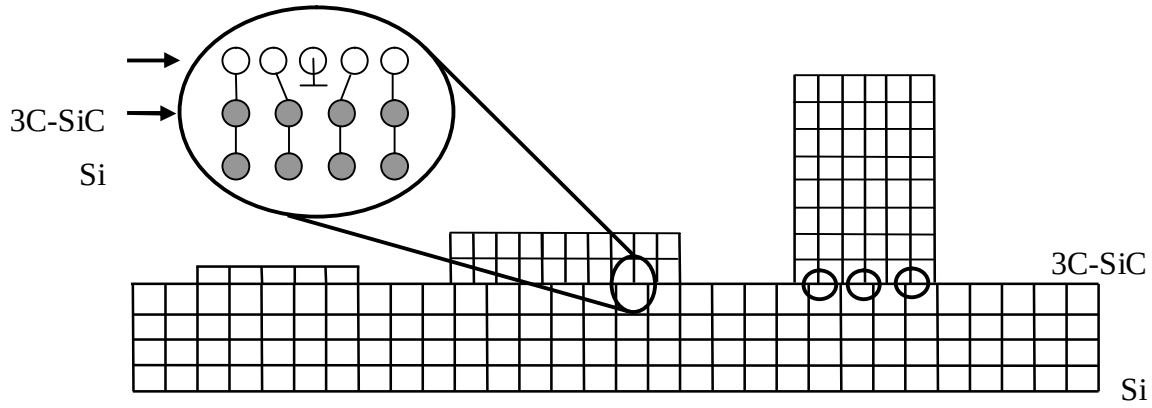


Figure 1.1 Illustration of the effect of lattice mismatch in heteroepitaxy. The ⊥ symbol denotes the location of a missing row of atoms which is known as a line defect. Note the stretched and compressed covalent bonds at the interface resulting from the lattice mismatch between the two crystals. [ref]

As seen in the above figure, there is a strain in the epilayer from an attempt by the epilayer ($a_{3C\text{-}SiC}$ = 4.3596Å) to accommodate the substrate's lattice constant (a_{Si} = 5.43095Å) (Harris 1995). The attempt to accommodate the mismatch not only produces crystal defects, but these defects in the epitaxial layer have a mosaic morphology in the case of the (100)3C-SiC/(100)Si system. While a carbonization step is normally employed which converts the starting Si surface to SiC and acts as a buffer layer to reduce the stress, this does not completely accommodate the lattice mismatch. With this buffer layer, there are still a fair amount of dislocations which must be reduced if 3C-SiC is to be useful for electronic devices such as MOSFETs.

One of the most successful methods to grow 3C-SiC is by chemical vapor deposition (CVD). The standard precursor chemistry typically used is the silane-propane-hydrogen gas system. Although extensive work has been performed since the early 1980's, there is still a lack of good quality 3C-SiC on Si epitaxial material. While

growth rates up to 40 μm/h on undulant Si (100) substrates by cold-wall CVD have been reported to produce SiC substrates with near bulk quality, defects originating from the undulant substrate persist (Nagasawa, Yagi and Kawahara 2002). More relevant for device manufacturing were studies performed using hot-wall CVD, which resulted in growth rates up to 50 μm/h (Reyes, spring MRS 2006). While these films were relatively flat (i.e., low residual stress) they were far from 'defect free' which is generally a minimum condition to allow for electronic devices to be successfully realized.

1.2.1 Why Heteroepitaxial Silicon Carbide?

Unlike the more commonly studied hexagonal forms of SiC, 4H-SiC and 6H-SiC, 3C-SiC has the ability to be heteroepitaxially grown on Si, allowing for the growth of SiC on large area substrates. Si wafers are inexpensive and are currently manufactured as large as 12 inches in diameter. 3C-SiC could be epitaxially grown on large-area Si wafers to produce seeds for bulk growth. Currently, only bulk SiC is available in the 4H and 6H polytype with boule sizes capable of producing a maximum 4 inch size wafer at a cost of nearly $2000-$2500 per wafer (Cree, Inc. 2009). Furthermore, bulk SiC grown by physical vapor transport contains screw dislocation densities near 10-200 cm^{-2} that can penetrate into the epitaxial layer during growth and lead to device failure. Because of the cubic crystal structure of 3C-SiC, these screw dislocations are energetically unfavorable and do not in occur in 3C heteroepitaxy.

Heteroepitaxy opens opportunities for silicon carbide growth on a variety of novel substrates in order to exploit or suppress certain attributes. In order to reduce the detrimental effects stemming from the coefficient of thermal expansion mismatch between SiC and Si,

3C-SiC has been grown on $Si_xGe_{(1-x)}$ substrates. 3C-SiC films have also been grown on silicon substrates patterned with inverted nanopyramids to successfully reduce defect propagation via defect annihilation within the films (D'Arrigo 2010), see Figure 1.2. Fabrication of devices, e.g. MEMS, can be facilitated by growing polycrystalline SiC on sacrificial oxide release layers by using a polysilicon seed layer. The oxide layer can be etched with hydrofluoric acid (HF) to release the patterned SiC MEMS structures. This avoids problems that silicon wet etchants may present when releasing SiC directly from a Si substrate- masking effects due to bubble formation on the substrate surface and the increased risk of structural damage due to agitation, especially with submicron thick films. The polysilicon seed-layer can be tailored to impact the grain characteristics of the poly SiC film, resulting in a highly-textured poly-SiC film (C. L. Frewin 2009). Indeed, this preliminary work was the motivation for this dissertation research where the next logical step was to realize MEMS devices on the poly-SiC on oxide wafers.

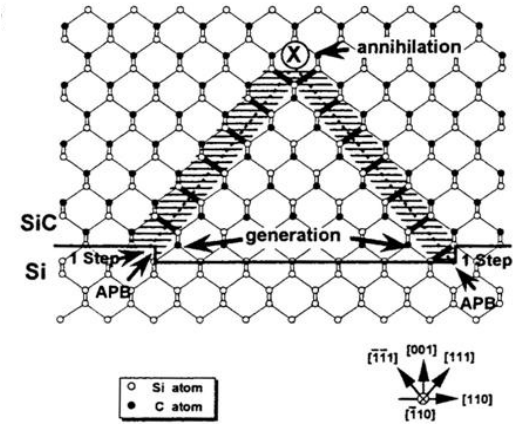


Figure 1.2 Schematic representation of antiphase domain boundary (APB) annihilation with film thickness. The solid line represents the Si-SiC interface. Note that the APBs form at the atomic steps of the Si surface. (Mendez, et al. 2005)

1.2.2 Fabrication of Silicon Carbide MEMS

Although the micromachining of single-crystal bulk silicon carbide, i.e. 4H-SiC and 6H-SiC, has been demonstrated using SiC-epi on SiC bulk substrates to produce pressure sensors (Okojie 1996), heteroepitaxial SiC has the advantage of being grown on relatively inexpensive, high quality, large area Si substrates and readily processed using many of the conventional Si bulk micromachining techniques. The high etch resistance of silicon carbide to the wet chemistries used to process Si and SiO_2 allows SiC to act as an etch stop during a broad range of processing steps. Figure 1.3 shows a process flow demonstrating the realization of diaphragm and cantilever structures from epi-SiC on Si. In the case of the backside etch, the SiC membrane serves as an etch stop to provide excellent thickness control of the membrane. Freestanding SiC microstructures, like the cantilever shown in Figure 1.3, are first patterned using dry etching (plasma) and then the structure is released by etching the bulk silicon with an anisotropic wet etchant, e.g. KOH, TMAH, or EDP.

As previously mentioned, wet etching isn't practical to use to pattern silicon carbide, so plasma etching techniques have been developed. The fluorine-based plasma chemistries developed for the etching of Si, SiO_2, and Si_3N_4 are also used for SiC. SF_6, NF_3, CHF_3, and CF_4 are commonly mixed with O_2 at pressures below 200 mTorr to promote reactive ion etching and suppress sputtering of the substrate (M. Z. Mehregany 1998). Although, the oxygenated plasmas quickly erode common photoresist masks, photoresists, such as AZ® 4620 manufactured by AZ Electronic Materials, are available that are resistant enough against erosion in fluorine-based plasmas to serve as a dry etch soft mask. Photoresist masks can exhibit etching selectivity up to 1:1, which is fine for

patterning larger feature sizes (≥ 4μm) or processing thin SiC films. However, aluminum or nickel hard masks are preferred for patterning SiC in etching plasmas since only thin metal coatings are needed owing to the high selectivity of the metal films (1:40 for Ni on 3C-SiC). Nevertheless, aluminum hard masks are prone to an effect called micromasking, a phenomena that occurs when sputtered atoms from the metal mask deposit on the surrounding etch field and masks the undying material of the etch field. Grass-like structures result if the etching environment has a high-degree of anisotropy. The addition of small amounts of hydrogen to the gas mixture reduces this effect (M. Z. Mehregany 1998).

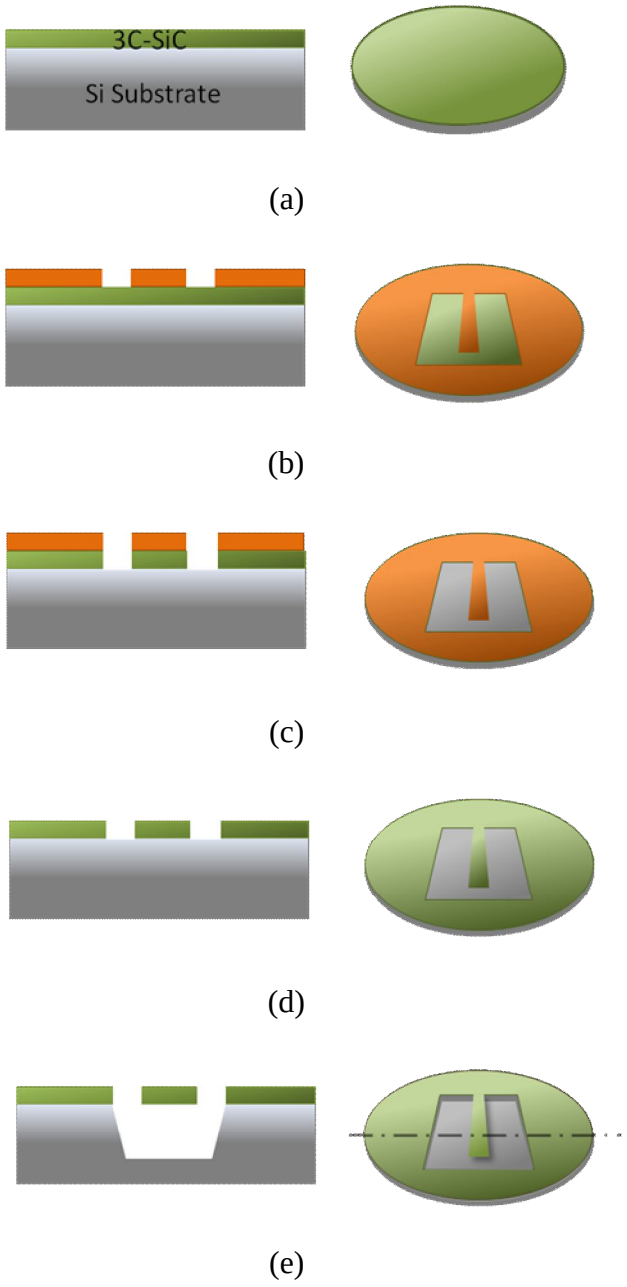


Figure 1.3 Fabrication of a free-standing cantilever. (a) CVD growth of 3C-SiC film on a Si substrate. (b) Mask material (shown in orange) is spun (photoresist) or deposited (metal) on the wafer and then patterned. (c) The 3C-SiC is dry etched using SF_6/ O_2 plasma. (d) Mask layer is removed. (e) Structure is released by etching the underlying silicon with a heated 20% KOH solution.

Surface micromachining is a process in which sacrificial thin films are used as a platform for the deposition of a structural layer, but are then removed to release a freestanding MEMS structure. Silicon bulk micromachining techniques can be used for processing monocrystalline, polycrystalline, and amorphous SiC, however, conventional surface micromachining is currently only possible with poly and amorphous SiC. Polycrystalline SiC structural layers can be deposited on a poly-Si or SiO_2 sacrificial layer to exploit the fact that SiC is highly resistant to Si and SiO_2 etchants. When poly-Si is used as a sacrificial layer, a thin oxide layer is used to protect the underlying Si substrate during the release of the structure from the sacrificial layer. Poly-SiC grown on SiO_2 and Si_3N_4 films tend to form randomly-oriented, equiaxed grains. In contrast, the crystal grains of the poly-SiC film grown on poly-Si matches the textured grains of poly-Si, forming a polycrystalline epitaxy (Zorman 1996). This suggests that one could vary the microstructure of the SiC film to tailor the device's performance by selecting the appropriate poly-Si substrate deposition conditions. The work discussed in this dissertation explores the influence of thickness-dependant microstructure changes (i.e. grain size and grain texture) of thin polysilicon films on the SiC film.

1.2.3 Stress-Induced Deformation of Heteroepitaxial Films

As discussed earlier, heteroepitaxial SiC offers several benefits over bulk-grown SiC since heteroepitaxial SiC can be incorporated into current silicon processing technology and a variety of substrates can be implemented to suit design/ fabrication needs. Unfortunately, the heteroepitaxial growth of 3C-SiC on Si is exacerbated by a 20% lattice mismatch and 8% coefficient of thermal expansion (CTE) between Si and 3C-SiC

(refer to Table 1.1), which leads to in-plane stress within the film. The stress that develops within the SiC film near the SiC-Si interface is tensile, resulting in concave bowing of the wafer or, in the case of growth on (111)Si substrates, film delamination and cracking. Often the atomic bonds along crystal planes will break and reform to relieve film stress, leaving behind dangling bonds which are referred to as misfit dislocations (Smith 1995). At the edge of the wafer or areas where the film-substrate system terminate, deformation of the film edge will occur due to the film being "pinned" at the film-substrate interface, refer to Figure 1.3(a). This deformation will cause out-of-plane bending of free-standing structures As the film grows, a stress gradient parallel to the direction of growth frequently develops within 3C-SiC films, causing out-of-plane deformation of released structures, Figure 1.3(b). These material growth-related issues need to be addressed before 3C-SiC can be realistically considered as a replacement for Si-based MEMS device structures.

1.3 Polysilicon-on-Oxide Substrates for Heteroepitaxial Silicon Carbide

SiC is a semiconductor material that is desirable for many power electronics and MEMS applications due to its wide band gap, mechanical resilience, robust thermal properties, and chemical inertness. However, many of these inherent properties create extreme difficulties when processing MEMS devices with this material. SiC chemical resistance reduces the effectiveness of wet chemical etching and requires the use of dry etching techniques involving reactive ion etching (i.e., DRIE/RIE). Fortunately, 3C-SiC, can be grown heteroepitaxially on Si substrates, and the addition of this Si layer allows for many more processing options in device manufacturing. For example, one can utilize the Si substrate as a sacrificial layer for the creation of freestanding 3C-SiC MEMS structures (Beheim and Evans 2006) (Carter, et al. 2000). However, the recipes used to

etch Si in DRIE/RIE have a similar etch rate with SiC, thereby excluding selectivity and reducing accuracy for the desired structure (Beheim and Evans 2006) (McLane and Flemish 1996) (Rosli, Aziz and Hamid 2006). Freestanding SiC MEMS devices using sacrificial Si layers have also encountered difficulties during device fabrication resulting from unetched Si preventing the complete release of the structure (Beheim and Evans 2006) (Carter, et al. 2000). Silicon dioxide, SiO_2, has been traditionally used as an etch-stop in Si processing involving DRIE/RIE, and can be easily removed by wet chemistry processes to allow for the full release of freestanding structures (Federico, et al. 2003). With this in mind, silicon-on-insulator, SOI, substrates provide an excellent media for the creation of freestanding SiC devices by providing not only an oxide for the etch-stop for DRIE/RIE, but also a Si crystal seed layer for the heteroepitaxial growth of the 3C-SiC (Shimizu, Ishikawa and Shibata 2000) (Myers, Saddow, et al. 2004).

SOI provides some additional benefits for the growth of 3C-SiC as shown in previous studies (Shimizu, Ishikawa and Shibata 2000) (Myers, Saddow, et al. 2004). The high temperatures required for the growth of single-crystal 3C-SiC soften the SiO_2 layer, allow dispersion of stress caused by the ~20% lattice mismatch between SiC and Si, and suppress the formation of voids caused by Si evaporation at the 3C-SiC/ Si interface (Carter, et al. 2000). Although thick SOI seed layers (>50 nm) have been shown to produce 3C-SiC films that are of comparable quality when compared to 3C-SiC films grown on single-crystal Si substrates, the benefits of the epitaxial growth of 3C-SiC on SOI are realized when 3C-SiC is deposited on a thin (<50 nm) seed layer of Si, which produces excellent quality 3C-SiC (Shimizu, Ishikawa and Shibata 2000) (Myers, Saddow, et al. 2004). However, a major drawback of using SOI in the production of 3C-

SiC devices is the fact that it requires extensive processing techniques (Shimizu, Ishikawa and Shibata 2000) (Myers, Saddow, et al. 2004). These processes add to the overall production cost of the device. In addition many MEMS devices do not require single-crystal SiC material for proper functionality. A cost-efficient, easily produced wafer stack consisting of poly-Si/ SiO_2/ Si layers could replace the SOI substrate if poly-SiC is desired as a material for MEMS applications.

The SiC Group at the University of South Florida has been investigating the optimization of the new process of growing thin-film 3C-SiC on a thin (≤ 100nm) polycrystalline Si (poly-Si) seed layer. The poly-Si is CVD-deposited on a CVD-deposited SiO_2/ Si (111) stack and poly-3C-SiC is formed on this poly-Si seed layer. The CVD deposited poly-Si seed layer appears to exhibit a highly-textured grain structure, in other words, the polycrystalline grains are oriented in a preferred direction. The texturing of the poly-Si layer is very sensitive to its deposition temperature. It is reported that the films are deposited favoring the <110> orientation and, once annealed, tend to arrange in the <111> orientation (Parr and Gardiner 2001). Growing the 3C-SiC via the poly-Si seed layer on an oxide release layer will provide a versatile substrate for the fabrication of free-standing, highly-crystalline 3C-SiC MEMS structures with low residual stress.

1.4 Influence of Polysilicon Seed-Layer Thickness on Silicon Carbide Film Stress

The behavior of polycrystalline films is largely determined by the grain morphology and the general orientation of the crystallites within the film (i.e., film texture). Smaller grain size, especially when they exhibit columnar structure, usually results in a higher concentration of small angle grain boundaries. These boundaries tend

to be areas of lower density and the interatomic forces within the boundary try to close the gaps, which results in a tensile stress on the surrounding crystallites (Koch 1994). Polysilicon films deposited at temperatures ≥ 610°C form a conical grain structure and exhibit compressive stress (Parr and Gardiner 2001). The origin of the compressive stress is not well understood, but is believed to be a result of hydrogen incorporation into the growing film (Yu et. al) or the insertion of excess adatoms into the grain boundaries (citation). Early in the deposition small, randomly oriented grains grow and compete with one another depending on their orientation with respect to the growing film. Crystallites oriented for fast vertical growth will out-compete slower growing misoriented grains. This results in fewer, but larger, conically shaped grains as the film grows (see Figure 1.5). Compressive polysilicon films tend to exhibit positive stress gradients and, as a result, curl upward when released from the substrate (Madou 2002).

Silicon carbide films were grown on polysilicon seed layers deposited under conditions which favor cone-shaped grain growth and compressive intrinsic stress. Cantilevers fabricated from 3C-SiC films grown on a ~20nm thick polysilicon layer demonstrated a positive gradient stress, i.e. upward curl, whereas cantilevers fabricated from 3C-SiC films grown from a ~100nm polysilicon seed-layer developed a negative gradient stress, i.e. downward curl. Surface probe analysis of the polysilicon layers revealed substantial size and morphology differences of the surface structure of the gains. Transmission electron microscopy (TEM) of the 3C-SiC film grown on the 100nm thick polysilicon seed-layer showed relatively well-ordered grains near the SiC-Si interface with increasing randomness of the grain orientations away from the interface.

1.5 Overview of the Organization of This Dissertation

SiC demonstrates roboust electrical, chemical, and mechanical performance suitable for use in harsh environments where Si-based MEMS devices would fail. Unfortunately, the chemical inertness is a desirable property for device application; it presents challenges for the processing of heteroepitaxial SiC films. Coupled with the inherent problems of heteroepitaxial growth, new techniques to reduce or eliminate these issues must be investigated if SiC is to be realized as the preferred fabrication material for harsh environment devices. Chapter 2 will discuss the principles of CVD growth and hardware, since chemical vapor deposition is the primary means of growing 3C-SiC. An overview of crystal defects and polycrystalline film growth as they apply to heteroepitaxial growth of 3C-SiC on Si will be then be presented. The chapter will conclude with a mechanical analysis of thin film stress. Chapter 3 will discuss the first experiments to realize high-quality poly-3C-SiC films on poly-Si on oxide wafers. Chapter 4 presents the first experiments aimed at producing MEMS structures on the poly-3C-SiC on oxide layers developed and presented in Chapter 3. Based on the lessons learned in this phase of the research the MEMS structures were re-designed so that stress-strain information could be extracted directly from the released MEMS structures. Finally, Chapter 5 will discuss future research exploring post fabrication annealing of MEMS structures micromachined from the stoichiometry-dependent bilayer film and further characterization of the microstructure of the polycrystalline SiC films.

CHAPTER 2: HETEROEPITAXIAL SILICON CARBIDE STRUCTURE, GROWTH, AND THIN FILM MECHANICS

2.1 Crystal Structure of Silicon Carbide

Silicon carbide can exist in many different crystal structures depending on growth conditions, a phenomenon called polytypism. Polytypism is a special case of polymorphism, in which the crystal structures between two polymorphs differ only in the way identical, two-dimensional layers of close-packed layers are stacked. In the case of SiC, polytypes vary by the different stacking sequences of the tetragonally-bonded Si-C subunits, with more than 220 polytypes known to exist (Foll 2006). However, an overwhelming majority of electronic materials research is concerned with only three of these polytypes: 4H-SiC, 6H-SiC, and 3C-SiC. The 4H, 6H, and 3C designation, called the Ramsdell notation, is the most wide-spread method of identifying polytypes (Foll 2006). The number-letter prefix designates the quantity of close-packed Si-C layers required for each unit cell and whether the polytype is a hexagonal (H), cubic (C), or rhombohedral (R) crystal system. For example, 4H-SiC indicates a hexagonal crystal system comprised of a repetitive, uniquely-ordered stacking sequence of four (4) Si-C subunit layers.

The hexagonal close-packed structure is a main reason for the high stability of the hexagonal SiC polytypes. The 4H-SiC polytype has the highest stability due to the

alternating cubic and hexagonal layers (Park, et al. 1994). 6H-SiC has a low, anisotropic electron mobility, while 4H-SiC has a much higher electron mobility and is less anisotropic, i.e. less directionally dependent (Casady and Johnson 1996). Thus 4H-SiC is, at present, the most commonly used polytype for electronic devices (Saddow and Agarwal 2004).

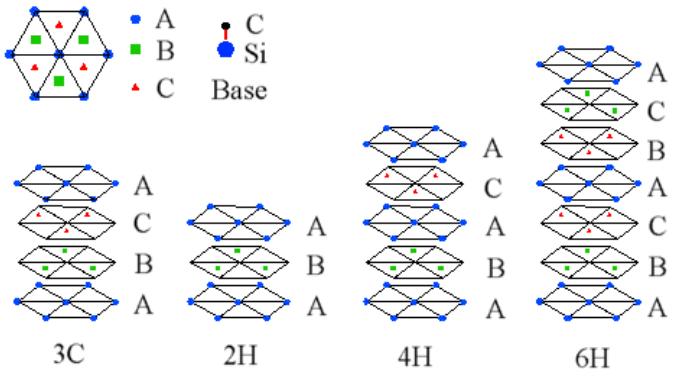


Figure 2.1 Four examples of SiC polytype stacking sequences. Each point represents a lattice point on which the Si-C basis is attached. Each layer is the close packed plane of the crystal system and is differentiated by "A", "B", or "C", which is determined by the relation of each layer's lattice point positions to the interstitial spaces of the other layers (Saddow and Agarwal 2004).

The 'A', 'B', and 'C' labels in Figure 2.1 denote the position of the lattice points, a collection of periodic points in space, on which the Si-C subunits are located. As seen in Figure 2.1, 4H-SiC has a stacking sequence of ABCB, or 4 layers, therefore the designation is 4H. This structure has an equal number of cubic and hexagonal lattice sites. The 6H-SiC structure has 6 stacking layers before the sequence repeats ABCACB, and, finally, 3C-SiC is a continuation of the ABC stacking sequence which has purely cubic symmetry. Due to differences in stacking sequence, the electrical, mechanical and optical properties vary for each polytype of SiC, as shown in Table 1.1.

2.2 Overview of CVD

Chemical vapor deposition (CVD) is a technique in which a solid film is formed onto a surface by a chemical reaction emanating from vapor phase precursors. The chemical reactions generally undergo activation by ohmic heating, RF induction heating, plasma, or light. It is a technique often employed for the uniform growth of high quality thin films. The common types of CVD are 1) Organometallic Vapor Phase Epitaxy (OMVPE) 2) Plasma Enhanced Chemical Vapor Deposition (PECVD) 3) Photo CVD 4) Low Pressure CVD and 5) Atmospheric Pressure CVD. Chemical vapor deposition involves a series of sequential steps beginning with the vapor phase and progressing through a series of quasi steady-state reactions which culminate in the development of a sold film. The progression from vapor phase to film growth can be summarized by the following sequence of events. First, the gaseous reactants diffuse through the stagnant fluid layer (i.e. so called 'boundary layer') to the growth surface. Second, the reactants adsorb on the surface and then usually undergo some surface migration to reach a reaction site (i.e., dangling chemical bond). Third, the reactants undergo a chemical reaction which may be catalyzed by the surface. Fourth, the reaction by-products undergo desorption from the surface. Fifth, the reaction by-products diffuse through the boundary layer, enter the gas stream and are exhausted out of the reactor. Finally, the condensed product is incorporated into the structure of the developing film. The process is summarized in Figure 2.2 below.

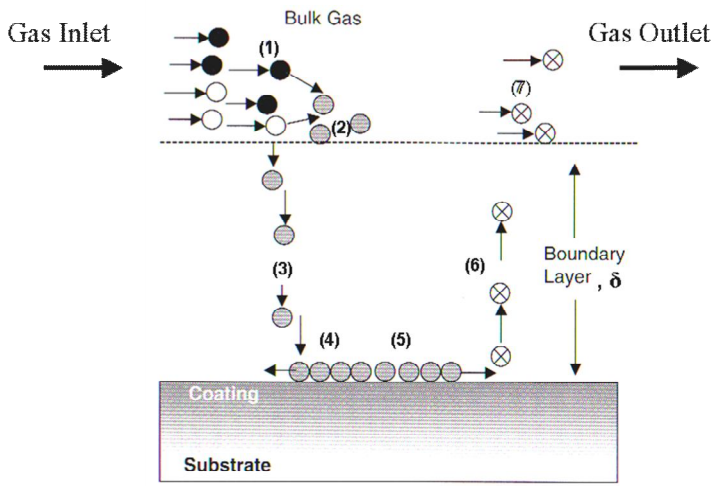


Figure 2.2 Schematic diagram of mechanistic steps which occur during the CVD process. (1) Gas inlet, (2) dissociation of reactants, (3) diffusion of reactants to the surface, (4) adsorption of reactants to the surface, (5) heterogeneous surface reaction, (6) desorption of by-products, (7) diffusion of by-products back into the bulk gas (Park and Sudarshan 2001).

Although many rate-limiting steps are known to exist, the deposition rate of CVD processes is primarily governed by two mechanisms: mass transport and surface kinetics. These two rate-limiting steps are influenced by several process parameters. The temperature and pressure of the reaction environment greatly impact the deposition process. The pressure controls the thickness of the boundary layer and, as a result, affects the rate of the reactant and product diffusion (Sivaram 1995). At low pressures, the boundary layer is thinner, which minimizes the diffusion time across the region. This is known as the reaction-rate-limited CVD regime; where the rate of deposition is limited by the reaction rate of reactants on the surface and is more sensitive to temperature (Sivaram 1995). If the temperature is low, then an oversupply of reactants is created due to the molecules reacting slowly (Sivaram 1995). If the temperature is high, then the surface reactions take place quickly and the reaction rate is limited by the diffusion of

molecules. This is generally the case for high pressures as the boundary layer is thicker and diffusion becomes the rate-limiting step. The growth regime (transport-limited or surface reaction-limited) is determined by the slowest process (diffusion or chemical reaction) (Smith 1995). Figure 2.3 illustrates how both the temperature and pressure during CVD affects the growth rate.

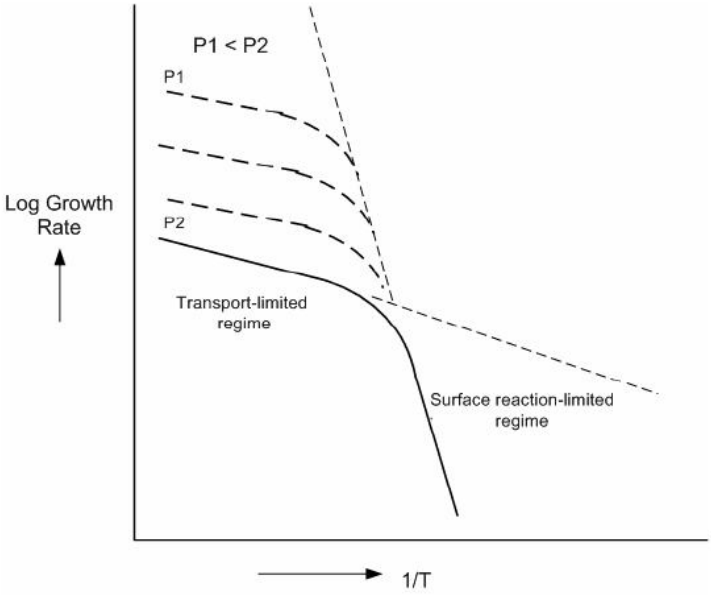
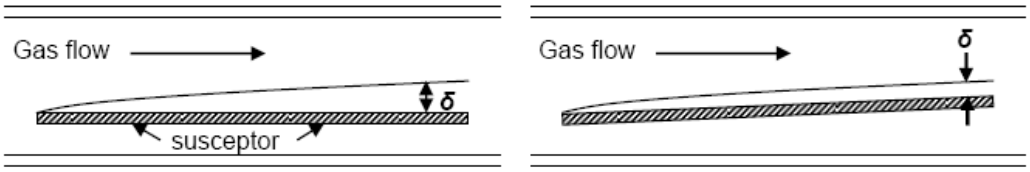


Figure 2.3 Generalized process trend showing the dependence of process temperature and pressure on growth rate via CVD (Smith 1995).

Another important process parameter that influences reaction rate is gas velocity. The CVD process involves the transport of precursor gases through the use of a carrier gas, which is designed to flow in a laminar manner although occasionally some turbulence is present (Park and Sudarshan 2001). When a fluid flows over a stationary surface, a thin layer of fluid immediately above the surface is stationary. This is known as the boundary layer, as stated above, and is inversely proportional to the gas velocity

and directly proportional to the fluid viscosity and pressure. In a horizontal CVD reactor design, the boundary layer increases along the direction of the carrier gas flow (as the temperature of the gas increases), which leads to an exponential decrease in the deposition rate. Tilting the susceptor increases the gas velocity by continuously decreasing the cross-sectional area and thus reduces the thickness of the boundary layer along the flow direction (Rossi 1988). Figure 2.4 illustrates these principles.



(a) (b)

Figure 2.4 Illustration of the boundary layer, δ, in a horizontal reactor with: (a) flat susceptor design, and (b) tilted susceptor design (Pierson 1999).

2.2.1 Early Stages of CVD Film Growth

The initial stages of film growth are characterized by three major phenomena which occur independent of the type of film growth technique. The material first condenses out of the vapor phase and nucleates on a substrate. This condensation process begins with the reactant species impinging on the surface and bonding to the substrate atoms at the gas-substrate interface. The probability that an impinging atom will be adsorbed onto the surface is related to a quantity called the sticking coefficient, which is the ratio of the amount of material condensed on the surface to the total amount of impinging atoms, Figure 2.1 (Sivaram, S 1995). Once an atom is adsorbed onto the surface it must overcome a surface binding energy, Q_{desorb}, in order to leave the surface.

Given the vibrational frequency, ν, of the adsorbed atom, the length of time, τ_s, which an atom stays on the surface, is expressed by:

$$\tau_s = \left(\frac{1}{\nu}\right) \cdot \exp\left(\frac{Q_{desorb}}{kT}\right) \tag{2.1}$$

When Q_{desob} is large in comparison to kT, the adsorbed atom will spend a long time on the surface, so the chance of the atom being incorporated on the surface is high (Sivaram, S 1995). When the energy of the surface atoms is on the order of kT, then the adsorbed atom will have a high probability of being desorbed. Once incorporated onto the surface, the condensed atoms or molecules tend to aggregate and form small clusters on the surface of the substrate, a process called nucleation. These small clusters are in a constant free energy struggle between the releasing of free energy when forming a cluster and having to pay an energy cost when forming a surface interface between two distinct phases. Small clusters are unstable if the energy released from the formation of its volume cannot sustain the creation of its surface. Once the clusters have reached a critical size, any addition of molecules to the cluster releases energy instead of costing energy and nucleation growth can be sustained. Then the randomly formed nucleation sites reach a saturation density and undergo island coalescence via the diffusion and continuing capture of adatoms. This saturation point occurs when the internuclear distances are on the order of the mean surface diffusion length. As the islands grow, they assimilate subcritical nuclei and coalesce with other islands, forming a connected network. Eventually, the steady-state growth above the first layer occurs. However,

CVD processes add an additional step to the film growth process; a chemical reaction among the surface-adsorbed reactants occurs at the gas-substrate interface. Whereas simple condensation is always exothermic, a majority of CVD reactions are endothermic which means they must usually wait until they interact with the heated substrate. Another important feature of the CVD process that complicates this general growth sequence is that the intrinsic impurities, in the form of reaction products, need to be considered in the vicinity of the film growth (Sivaram, S 1995).

2.3 Overview of Heteroepitaxial Defects

Given the nature of heteroepitaxy, i.e. growing a crystalline material on a different crystalline material (substrate), it is nearly impossible to generate a perfect, mono-crystalline film. Other than the introduction of impurities from contamination, the common source of extrinsic crystal defects found in heteroepitaxy stems from a mismatch between the lattice constant and the coefficient of thermal expansion between the substrate and film. These disparities create line defects, such as dislocations, or planar defects as is the case for micro-twins, stacking faults, and grain boundaries.

2.3.1 Line Defects

Dislocations are linear defects resulting from the deviation of atoms from the lattice site positions of the crystalline structure. The disruptions of the atomic arrangement associated with dislocations typically extend through the structure along a line. Dislocations that commonly occur in heteroepitaxy are of the edge and misfit type.

Edge dislocations can be thought of as a disturbance originating from the insertion or removal of a partial plane of atoms from the crystal structure. The region at the end of the partial plane, where the atomic arrangement maximally deviates from the normal lattice sites, is called the dislocation line. The surrounding region is the dislocation core, which is an area of large strain and dangling bonds that runs alongside the dislocation line. The energy of propagation for an edge dislocation is much lower than the total bond energy of the atoms lying in the propagation plane. This is explained by the fact that an edge dislocation proceeds through a crystal peristaltic fashion. At any given moment, only one bond is broken while the atoms surrounding the dislocation are distorted from their equilibrium positions.

Another type of dislocation that is closely related to the edge dislocation, but is not seen in 3C-SiC heteroepitaxy, is the screw dislocation. This dislocation is often thought of as a crystal system which has been subjected to shear stress sufficient enough to overcome the elastic limits of the crystal. The result is the shifting of one side of the crystal relative to the other side by one or more lattice constants. In this case, the dislocation line runs in the direction of the shift. Referencing the atoms located within a plane perpendicular to the dislocation line, if an attempt is made to form a closed path around the dislocation line by connecting the atoms together, a helix will be formed. The once parallel planes of the crystal are now joined by a helical path; this is why this type of dislocation is referred as a screw dislocation. Although this dislocation is not seen in as-grown crystalline 3C-SiC films, its introduction is important for the understanding of grain boundaries.

Heteroepitaxial dislocations, called misfit dislocations, form at the interface of two crystals with different lattice constants. In an attempt to minimize the interatomic bonding strain induced by the lattice mismatch, the atomic planes of the thin film will be distorted at the interface and will no longer be equally spaced. The roughly equidistant points along the interface where the lattice deviations are the greatest correspond to the misfit dislocations. If the heteroepitaxial film has a coefficient of thermal expansion different than the substrate, then when temperature changes occur, usually during post-growth cooling, misfit dislocations occur in order to relieve in-plane stress present near the film-substrate interface.

2.3.2 Planar Defects

Planar defects correspond to disturbances of the crystal structure resulting from the two dimensional deviation of atoms from their corresponding lattice sites. Planar defects commonly found in heteroepitaxial films are stacking faults (SF), microtwins, antiphase boundaries (APB), and double position boundaries (DPB).

Stacking faults occur when a mistake occurs in the stacking sequence of the planes of atoms along certain directions. If planes of densely-packed spheres (atoms) are to be stacked on each other, one finds that there are two sets of interstitial spaces to place the next densely-packed plane. As a result, it is possible to lay three planes in succession without the co-alignment of interplanar atoms. In a perfect crystalline structure, a stacking sequence will eventually repeat in a periodic fashion. The face-centered cubic (FCC) structure is created when the stacking sequence repeats as ABCABC…and the hexagonal close packed (HCP) structure is created from the sequence ABABAB… In the

case of the zinc blende structure of 3C-SiC, it is not unusual to see stacking errors occur in the stacking of the {111} planes since the nearest-neighbor bonding is not affected by stacking faults. In fact, the energy associated with stacking faults is very low when compared to other planar defects since the defect is only due to the nearest-neighbor arrangement and not disturbances of the crystal structure. This mistake may arise during the film growth or when plastic deformation has occurred to the film. Figures 2.5 and 2.6 show a plan-view and cross-sectional TEM micrograph of the stacking faults present in a 3C-SiC film grown heteroepitaxially on (100)Si.

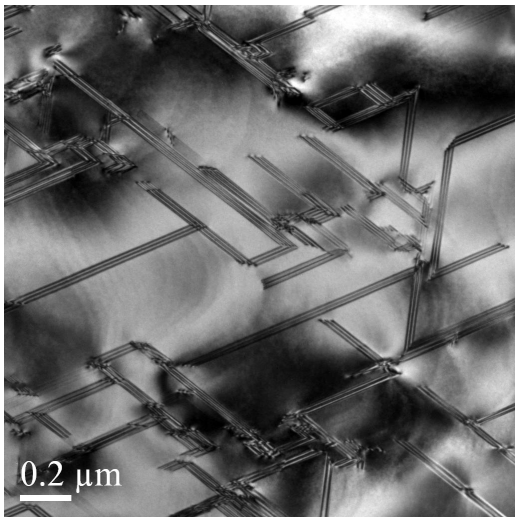


Figure 2.5 Stacking faults revealed in a (100)3C-SiC film via PV-TEM. SF density estimated to be ~ $5x10^4$ cm^{-1}. Data provided by C. Bongiorno, IMM-CNR, Catania, Italy.

Figure 2.6 Example of hetero defects in (100)3C-SiC from X-TEM. Note the defects along the (111) planes, also threading dislocations and stacking faults. Image courtesy C. Bongiorno, IMM-CNR, Catania, Italy.

Another type of planar defect resulting from the change of the planar stacking sequence is the micro-twin or, simply, twin. The distinctive feature of a twin is that the planar arrangements on opposite sides of the stacking disruption are mirror images of each other. For example, the stacking sequence ABCABCACBACBA…possesses a reflection about the A-plane located at the center of the palindrome. In the diamond or zinc blende structure, twinning occurs mostly about the (111) plane. Twinning causes a change in the crystal orientation. For crystal growth along the <111> direction in the zinc blende structure, the orientation of the crystal planes in the twinned region are along the <$\underline{111}$> or <115> direction. A very smooth surface morphology can result in 3C-SiC heteroepitaxial growth along the <111> direction since the twinning plane is the same as the growth plane. Figure 2.7 (a) shows a schematic representation of a micro-twin while Figure 2.8 shows a plan-view TEM micrograph of an actual micro-twin present in a 3C-SiC film grown on (100)Si.

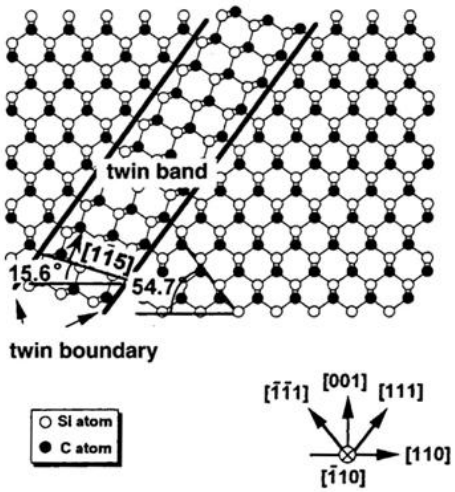


Figure 2.7 Schematic representation of micro-twin defect in SiC on Si heteroepitaxy. (Mendez, et al. 2005)

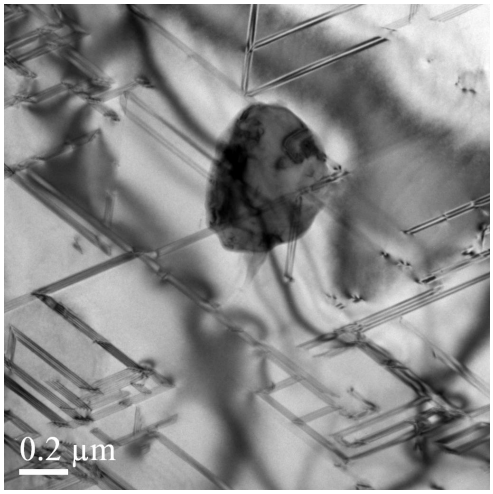


Figure 2.8 Micro-twinned crystal defect (dark cluster in center of micrograph) observed with plan-view TEM (PV-TEM). Data courtesy of C. Bongiorno, IMM-CNR, Catania, IT.

A planar defect that frequently occurs during the growth of (100)3C-SiC on (100)Si substrates is the antiphase boundary (APB). This type of defect is prevalent during APCVD growth and is significantly reduced at lower growth pressures (Cho and Carter 2001). The APB occurs when two islands having different ordered phase

coalesce. In the early stages of the film growth, partial surface steps may cause a relative position shift between the atomic stacking of different islands. In the case of SiC, due to surface roughness of the carbonized Si substrate, some islands of SiC may sit higher relative to others. As the islands grow and coalesce, a Si or C layer of one island may bond with another Si or C atom of another island forming a Si-Si or C-C bond as illustrated in Figure 2.9. These boundaries tend to propagate along the {111} planes (Ishida, Takahashi and Okumura 2003). However, the etching experiments of Li and Giling have shown evidence that APBs can propagate along the {110} plane (Ishida, Takahashi and Okumura 2003).

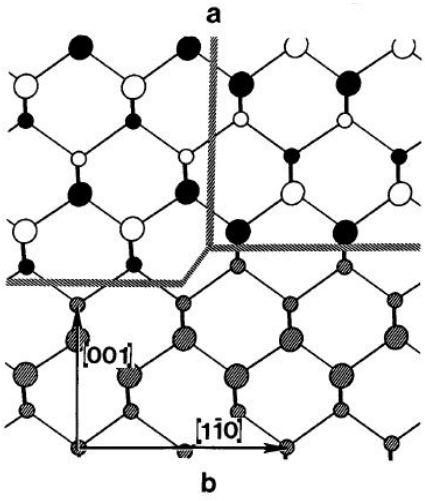


Figure 2.9 Geometrical consideration of the formation of an APB when SiC is grown on (100)Si substrate with an atomic step. Note the bonding of Si-Si and C-C atoms. (Cho and Carter 2001)

The double position boundary (DPB) is a special case of twinning in which separate domains are rotated about a 180° twin axis. This is seen when a FCC type crystal structure is grown in the (111) orientation on a (111) surface of a hexagonal crystal

(Kong, et al. 1987). This is commonly seen in 3C-SiC films grown on the basal plane of the hexagonal SiC polytypes. As illustrated in Figure 2.10(a), the (111) surface has two equivalent types of sites that the C atoms can locate. As a result, two different nuclei orientations can develop which are rotated 60° relative to each other. When these nuclei coalesce into each other, a DPB is formed. In Figure 2.10(b), the relative shift of the stacking sequence between neighboring domains is shown. The upper case "A" represents the surface of the substrate, while the lower case "a b c…" represents the stacking layers of the epitaxy. One can see that every third layer offers the opportunity to form a perfect bond across the interface, Si-C for example, the other planes cannot form this type of bond (Kong, et al. 1987). As a result, the boundary is somewhat disordered and the internal energy is high (Kong, et al. 1987).

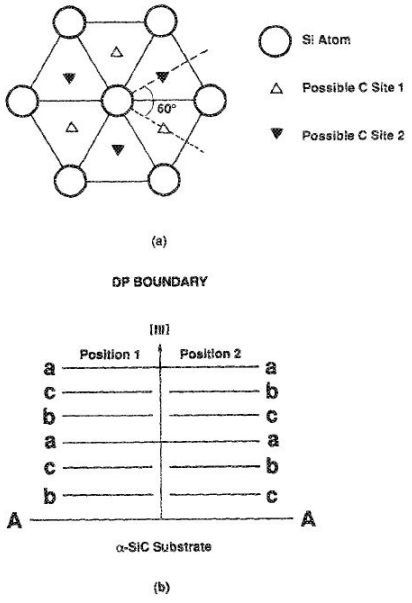


Figure 2.10 Stacking fault generation schematic showing the error in crystal layer formation resulting in a stacking fault defect. (a) top view representation and (b) side view showing the plane stacking sequence (Kong, et al. 1987).

2.3.3 Grain Boundaries

Since this dissertation involves the growth and characterization of polycrystalline films, it is worth looking at the role grain boundaries play in polycrystalline systems. Polycrystalline materials consist of several small crystalline regions, called grains or crystallites, bonded together by crystallographically defective regions called grain boundaries. Grain boundaries are interfaces where two crystals having different orientations meet without a disruption in the continuity of the material (Hirth 1968). Grain boundaries are generally categorized as low-angle grain boundaries and high-angle grain boundaries. Low-angle grain boundaries can be viewed as being comprised of several distinct and isolated dislocations whose properties are directly dependent on the degree of misorientation, ($\leq 10°$). An idealized, simplified case of creating a low-angle grain boundary is through a tilt and twist.boundary.

In the case of a tilt boundary, the crystal lattice can be visualized as being bent by an applied force about an axis parallel to the boundary plane. To reduce the energy associated by the bending, one can insert a wedge into the crystal. Edge dislocations, which are an extra plane of atoms, act like an imaginary wedge. As the bending angle is increased, more dislocations must be incorporated into the deformation in order to reduce the energy of the deformation.

The twist boundary involves rotation about an axis perpendicular to the boundary plane. In order to minimize the energy associated with the twist, two sets of perpendicular screw dislocations need to be introduced into a plane to create localized distortions. Generally, grain boundaries are never a pure tilt or twist boundary, but a combination of the two. When the angle of misorientation becomes large, the

dislocations become numerous and begin to overlap each other creating a very disordered boundary region.

2.4 Structural Evolution of Polycrystalline Thin Films

Grain formation in polycrystalline films grown using CVD processes is sensitive to several parameters such as temperature, deposition rate, dopant concentration, pressure, and impurity concentration. The structures of polycrystalline systems usually are governed by complicated, materials-specific phenomena (Thompson 2000). The processes described in this section are simple, generalized trends of behavior for materials. Polycrystalline films typically begin with the nucleation and coalescence of individual crystal islands on a substrate, an overview of this process was discussed in section 2.2.1. Grain growth is largely driven by the minimization of the excess energy associated with the total grain boundary area; as the grain boundary area decreases, the grain size must increase. Grain structure formation can occur through two distinct evolutionary processes. In one case, the grain boundaries formed early after island impingement are immobile and grain growth proceeds from the epitaxial growth of columnar structures. As the film grows, the grains oriented with the faster growing facets favoring vertical film growth will out-compete slower growing, misoriented grains, Figure 2.11. Sometimes this is referred to as conical grain growth.

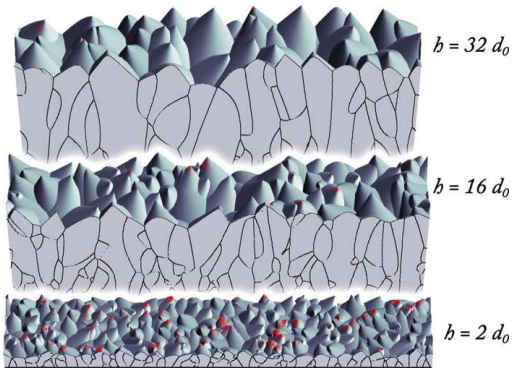


Figure 2.11 Evolution of grain structure with film growth. Cross-sectional slices of a simulated film at various thicknesses revealing grain evolution due to competitive grain growth among conical grains. The film thickness, h, is expressed in terms of the initial grain spacing, d_0. (Ophus 2010)

When the grain boundaries are mobile, the in-plane grain growth proceeds as the film thickens. The resulting grains appear to have an equiaxed, columnar shape that traverses the thickness of the film. As the film grows, the in-plane grain size increases with roughly the same scale. Often times, as unfavorable grain orientations are occluded due to competitive growth and the faster growing orientations drive film thickening, conical growth can lead to columnar grain growth with roughly parallel boundaries.

2.5 Mechanical Properties of Thin Films

While many thin film devices may be sought after for their electronic, magnetic, or optical properties, these devices are often limited by their mechanical properties. In the course of the deposition of thin films of materials, large stresses can develop, sometimes exceeding the tensile strength of the bulk material. These intrinsic stresses are often held responsible for the failure of thin film devices; in extreme situations the film may crack or peel from the substrate from where they are grown. From a technological point of view, it is important to understand the mechanisms responsible for thin-film

stress and develop methods to reduce or compensate for the impact these stresses have on thin-film bases devices.

2.5.1 Sources of Stresses in Thin Films

This section will open with a few distinctions that need to be introduced between widely employed and, occasionally misused, terminology. Stress, often denoted by the Greek letter, σ, is defined as the force, F, applied over a cross-sectional area, A, whose units are the same as pressure. It is simply expressed as,

$$\sigma = \frac{F}{A} \tag{2.2}$$

Strain, denoted by the Greek letter, ε, is a measure of a change of length, ΔL, arising from the displacement of a particle in a body based on a reference length, L. The length change may occur because of the application of an external or internal force, the expansion of a material from a temperature difference, etc. It is frequently expressed as a ratio,

$$\varepsilon = \frac{\Delta L}{L} \tag{2.3}$$

By convention, $\sigma > 0$ and $\varepsilon > 0$ are tensile stress and strain and $\sigma < 0$ and $\varepsilon < 0$ are compressive stress and strain, respectively. Residual stresses are those stresses that exist within a body when thermal gradients or externally applied loads have been removed.

Three sources of stress that can contribute to thin film's residual stress are intrinsic, epitaxial, and thermal.

Intrinsic stress refers to the collective stresses that develop during the growth of the film. It does not arise from the lattice mismatch or the thermal expansion-related strains of the film-substrate system, but occurs because of the film deposition process (e.g. nucleation, island coalescence, grain growth, film thickening, etc.), and develops under non-equilibrium conditions.

Epitaxial stress arises when a lattice parameter mismatch exists between the film and the substrate. This occurs when the film is very thin and there is coherency between the lattice sites of the film and the substrate. The misfit strain, ε_{mf}, by the distortion of the lattice spacing creates stress is given by

$$\varepsilon_{mf} = \frac{(a_s - a_f)}{a_s} \tag{2.4}$$

Where a_s and a_f are the substrate and film lattice constant, respectively. Once an epitaxial film reaches a critical thickness, t_c, the lattice becomes sufficiently strained and it becomes energetically favorable to form misfit dislocations in the film at the interface. The misfit dislocations introduce a stress field into the immediate area which relaxes the stressed interface. In the case of 3C-SiC, once the film grows past the critical thickness, 5 SiC lattice cells slightly exceed the distance spanned by 4 Si cells (i.e., 20% lattice mismatch). Sometimes epitaxial stress is lumped with other growth-related stresses as a

source of intrinsic stress but there is this fine distinction which is important to understand in order to try and reduce/eliminate.

Thermal stress is generated when strain is created from the material-dependent differential expansion between the film and substrate during a temperature change. This is often referred to as the Coefficient of Thermal Expansion (CTE). When the $t_f << t_s$, the stress is related to the strain in the film at a certain temperature, T, by:

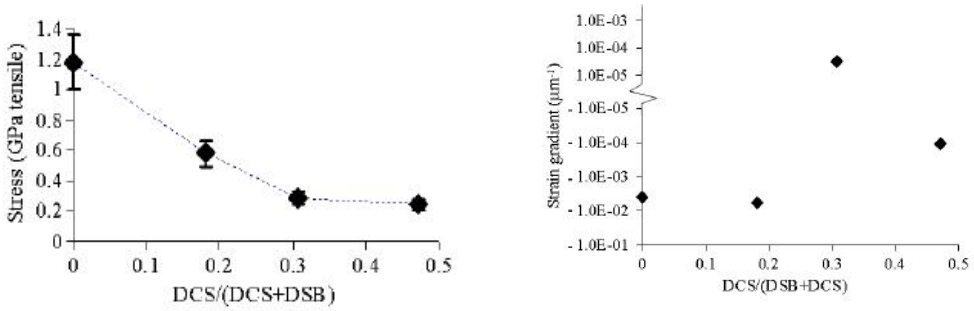
$$\sigma_{therm} = \left(\frac{E_f}{(1-\nu_f)} \right) \cdot (\alpha_f - \alpha_s) \cdot (T_{dep} - T) \tag{2.5}$$

Where E_f is the Young's modulus of the film, ν_f is Poisson's ratio of the film, α_f and α_s are the thermal expansion coefficients of the film and substrate, respectively and T_{dep} is the deposition temperature. In the case of SiC heteroepitaxy, the film is grown at temperatures usually exceeding 1300°C and then cooled to room temperature. The strain difference between the Si substrate and the 3C-SiC film due to this temperature-dependent contraction is nearly 8% and always results in a tensile ($\varepsilon>0$) thermoelastic strain in the 3C-SiC film.

2.5.2 Stress Control of Polycrystalline Silicon Carbide Films via CVD Process Parameters

It has been known since the early 1980's that Si-rich silicon nitride, Si_3N_4, thin films experienced stress relaxation when compared to fully stoichiometric Si_3N_4 (Habermehl 1998). By varying the ratio of dichlorosilane, $SiCl_2H_2$, to ammonia, NH_3,

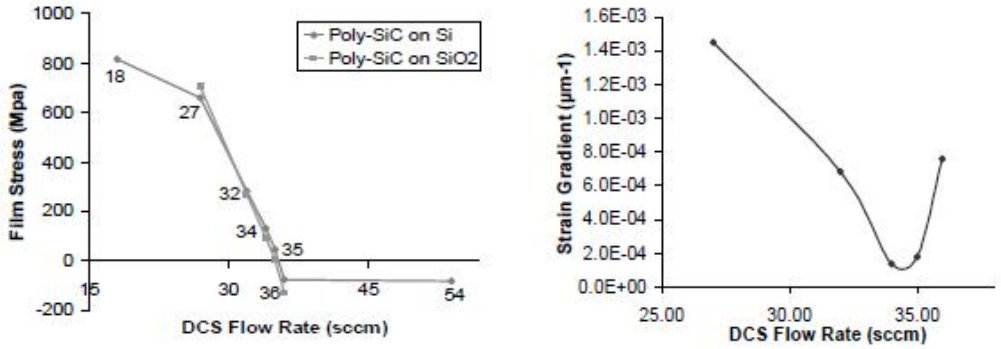
the residual film stress can be tailored from a high state of tension to one of compression for Si-rich films (Witczak 1994). Habermehl, reported that films with a silicon volume fraction of 10%-15% exhibited the lowest residual stress. A similar approach was adopted to control the residual stress and strain gradient of poly-SiC films deposited by regulating the fraction of dichlorosilane (DCS) relative to the total gas flow when using a DCS and 1, 3-disilabutane (DSB) precursor chemistry (Roper 2006). The reported growth rate for all films varied between 0.23µm/h- 0.32µm/h, generally increasing with the increase of DCS introduced into the gas flow. The Si:C ratio increased with the DCS flow fraction. The measured residual film stress and strain gradient decreased monotonically with increasing DCS fraction, see Figure 2.12(a) and 2.12(b) (Roper 2006). The stress reduction was attributed to the larger atomic radius of Si compared to C. The excess Si in the film increased the average bond length thus reducing the tensile stress.



(a) (b)

Figure 2.12 Relationship of the DCS fraction in the gas mixture to, (a) the residual film stress and, (b) the strain gradient (Roper 2006).

Results from the study of the average residual stress of poly-SiC films grown on (100)Si substrates (with and without SiO_2 thin film passivation) as a function of DCS flow were in agreement with the findings reported by Roper et al. (X. A. Fu 2009). The average residual stress and the strain gradient decreased in unison with increasing DCS flow fraction, both having coinciding minima at a DCS flow rate of 35 standard cubic centimeters per minute (sccm), see Figure 2.13. The increased presence of DCS in the gas mixture also increased the growth rate from 30Á/ min to 80 Á/ min. The inverse relationship between residual stress and growth rate has also seen in investigations studying the residual stress in poly-SiC films as a function of deposition pressure. These poly-SiC films exhibited a strong-texture in the <111> direction per XRD θ-2θ analysis.



(a) (b)

Figure 2.13 Results using DCS to control residual stress in poly SiC films. Influence of DCS flow rate on (a) the average residual film stress and, (b) the strain gradient measured from cantilevers fabricated from poly-SiC films (X. A. Fu 2009).

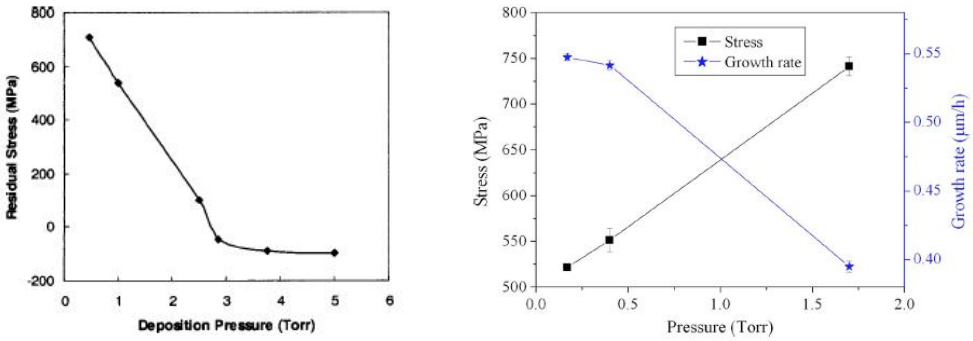
Polycrystalline SiC films grown on 100 nm thick polysilicon sacrificial layers deposited on thin Si_3N_4 exhibited a high degree of (111)3C-SiC texture and uniformity at the poly 3C-SiC/ poly-Si interface when a self-limiting carbonization step was incorporated in the deposition process. In contrast, poly-SiC films grown without the use

of a cabonization step exhibited voids at the poly-SiC/ poly Si interface, formed randomly oriented grains, had higher surface roughness and completely penetrated the unconverted polysilicon layer (Wiser 2003). Similar results were reported using thin polysilicon layers deposited on oxide to grow poly 3C-SiC that is highly textured in the <111> direction (Frewin 2009). The incoroporation of a cabonization step in the SiC deposition process allows the formation of a thin, usually <50nm thick, SiC layer that prevents the evaporation of Si at the higher temperatures used for 3C-SiC growth. Experimental evidence strongly suggests that the evaporation of Si is responsible for interfacial void and channel formation (S. E. Saddow 1999) . Poly-SiC will form on polysilicon via three-dimensional island growth using not only the Si from the source gas, but also from the underlying polysilicon as a result of thermally stimulated outdiffusion of Si and H_2 etching during the early stages of SiC growth (Wiser 2003). When two islands coalesce, vertical Si migration from the polysilicon layer may contribute to sizable cavity and void formation, structures that may contribute to intrinsic tensile stress within the SiC film.

Deposition pressure has been shown to have an impact on the residual stress and stress gradients in poly-SiC grown on (100)Si substrates (Fu 2004). The residual stress shifted from 710 MPa (tensile) to -98MPa (compressive) as the growth pressure was increased from 0.46 Torr to 5 Torr when grown using a SiH_2Cl_2 and C_2H_2 chemistry at 900°C, Figure 2.14(a). It was reported that cantilevers fabricated from the moderately tensile films exhibited a nearly-straight profile once released from the Si substrate, whereas the cantilevers fabricated from the compressive poly-SiC films bent upward. All the films exhibited columnar grain structure with strong (111)3C-SiC texture. However,

the films having high tensile stress contained a large number of high-angle grain boundaries with respect to the surface normal. In contrast, the microstructure of the compressive films exhibited columnar grain structure in which the boundaries were dominantly parallel to the surface normal.

Liu et al. used a methylsilane, SiH_3CH_3, and DCS precursor chemistry to grow poly-SiC on (100)Si substrates at 800°C to study the impact of deposition pressure on the residual film stress (Liu 2009). In contrast to the results reported by Fu, increasing the deposition pressure resulted in an increasing tensile film stress trend, Figure 2.14(b). Atomic force microscopy (AFM) revealed that the surface-projected grain size for the lower pressure growth was nearly twice the size of the higher pressure growth. The surface morphology certainly suggests that the increase of residal stress with respect to the deposition pressure may be due to grain boundary effects (Liu 2009). However, increasing the DCS flow fraction in the gas mixture also produced a decreasing tensile residual stress trend as reported by Roper et al. With increasing DCS fraction, the strain gradient changed from negative to positive, with the transition region coinciding with the minimum tensile residual stress.



(a) (b)

Figure 2.14 Residual stress versus deposition pressure trends for poly-SiC (Fu 2004) (Liu 2009).

The effect of deposition temperature on the residual stress was also investigated by Liu et al. using methlysilane as a single precursor source for poly-SiC growth on (100)Si substrates. Their results indicated a monotonic residual stress decrease from 1.4 GPa to 450 MPa as the growth temperature was increased from 700°C to 800°C at 170 mTorr, see Figure 2.15. The suggested growth rate plateau from 800°C to 850°C seems to imply that there is a transition from the surface kinetics limited regime (where the growth rate increased with temperature) to the transport limited regime (where the growth rate plateaued) (Liu 2009). XRD analysis of the resulting films exhibited several reflection peaks that implied the film grown at the lower temperature had a more randomly oriented grain structure than the films grown at the higher deposition temperatures.

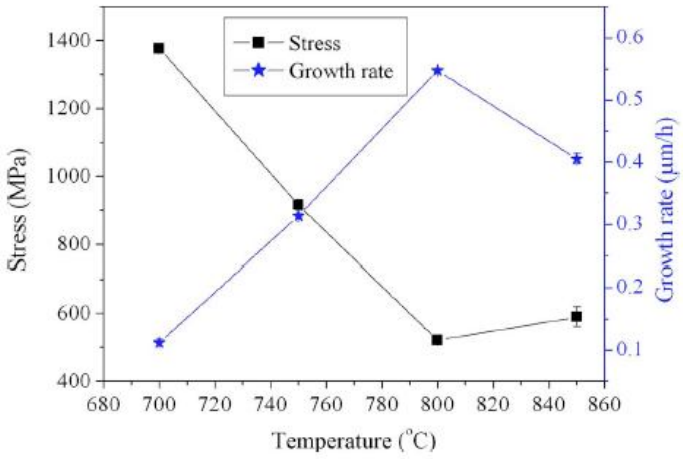
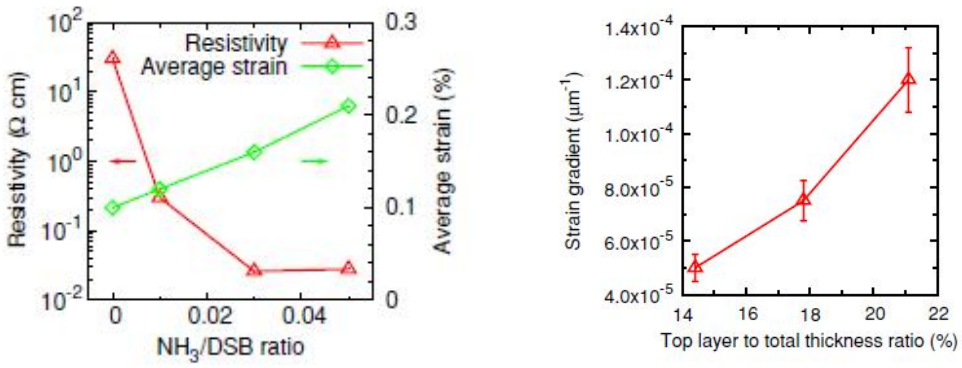


Figure 2.15 Poly-SiC residual film stress and growth rate vs. temperature at 0.17 Torr deposition pressure. Note the plateau after 800°C, which suggests that a surface kinetics-limited regime transitioning to a mass transport-limited regime (Liu 2009).

It has also been reported that poly-SiC films grown on oxidized (100)Si substrates exhibited residual stress that increased with deposition temperature using a tetramethylsilane, THS, single precursor source (Hurtos 2000). However, X-TEM analysis of the film-substrate revealed that the film grown at the lower temperature (1080°C) had a clearly-defined, intact oxide layer on which the columnar, (111) textured poly-SiC grew. The higher temperature deposition (1130°C) had no apparent oxide layer remaining and the poly-SiC film exhibited randomly-oriented, equiaxed crystallites. The deposition procedure incorporated high H_2 flow to avoid excess carbon in the films and was responsible for H_2-etching of the SiO_2 prior to growth. At 1080°C, the H_2 etching was not significant enough to remove the SiO_2 layer. However, at 1130°C the incomplete, or insufficient, removal of the oxide layer at the slightly higher deposition temperature appeared to have triggered the small grain size (Hurtos 2000).

An interesting approach to control strain gradients in poly-SiC thin films adopts a bi-layer structure using tailored N_2 doping during poly-SiC growth was investigated by Zhang et al. The technique is similar to the Multipoly process (J. H. Yang 2000), a process that has been used to create near-zero average film stress and near-zero stress gradients in poly-Si thin films. Alternate layers of compressive and tensile films are deposited by varying the deposition temperatures. (J. H. Yang 2000). However, since the Multipoly process is composed of stacks of partially amorphous and fully crystalline layers, long term stability issues may arise due to recrystallization (Zhang 2006). The DSB single prescursor is used as the Si and C source and ammonia, NH_3, is the doping source while all growths were carried out at 800°C. Uniform doping of the full film thickness was performed for varying NH_3 to DSB flow ratio from 0 to 5%. All films exhibited negative strain gradients (downward deflection) while the average film strain was tensile and increased from 0.10% to 0.21% when the NH_3/ DSB ratio was increased, Figure 2.16. N atoms occupy the C sites in the SiC lattice which causes the crystalline lattice to contract from 4.360 to 4.345Á, increasing the lattice mismatch between SiC and Si (J. H. Zhang 2006).



(a) (b)

Figure 2.16 The use of tailored N_2 doping during poly-SiC deposition to control film strain. (a) Relationship between average film strain and dopant concentration. (b) Strain gradient of a 3μm thick bilayer consisting of a 5% doped top layer and 3% doped bottom later as a function of the ratio between top layer thickness to the total thickness (Zhang 2006).

2.5.3 Analysis of Thin Film Stress

There are two principle methods that can be employed to assess the residual stress in thin films. The first is to measure the deformation of the substrate/film system using such means as a profilometer and then estimating the stress based on the radius of curvature. This is a 'as grown' technique that is frequently employed since it is not destructive and further film processing may be employed. The use of micro-raman spectroscopy which measures shifts in the transverse optical (TO) and longitudinal optical (LO) peaks can also be employed to determine film stress. In addition x-ray diffraction, in the so-called XRR (x-ray reflection) mode is often employed. However all of these microanalytical methods have limitations on their sensitivity and, ultimately one would like to assess the true mechanical properties of the stress in the film. This is particularly true for MEMS applications.

The second method to assess the residual stress in the thin film is to fabricate MEMS test structures and then carefully monitor the deformation/movement of these test structures as a function of film deposition properties. Clearly this second method is much more relevant to MEMS applications as one can have a true understanding of the actual film stress. However, this method is very time consuming and destructive. As a consequence the normal approach is to employ microanalytical methods first, track the stress level as a function of deposition conditions, and then use MEMS test structures to reveal the actual film stress. In this dissertation research this was the methodology employed, which is now discussed in further detail.

2.5.3.1 Stoney Equation

The establishment of a mathematical relationship between the residual stress present in the film-substrate system and the stress-dependent displacement of the film-substrate system, i.e. the Stoney Equation, is the goal of this section. Later, the relationship between the deflection of free-standing structures sensitive to uniform and gradient intrinsic stresses present in the film will be analyzed. Appendix A provides a brief introduction for those not familiar with the following derivation. It reviews the notation used in the following derivation and the mechanical analysis of a biaxially-deformed plate, the model that is the basis of the Stoney Equation derivation.

A stress-free film with a thickness, t_f, is bonded to a stress-free substrate with thickness, t_s, such that $t_s >> t_f$. The lateral dimensions of the film and substrate, L, is such that $L >> t_s$ and t_f. Figure 2.20 illustrates a series of steps depicting a way of creating a stressed thin film from a stress-free film-substrate system. First, it is imagined that the

stress-free film is removed from the stress free substrate and allowed to deform unrestrained by the substrate, Figure 2.17(a). Film stresses are caused by an elastic accommodation of an incompatibility between the film and substrate (Nix 2005). Second, after the film has deformed, external forces are applied to the film in order to deform the film in order to match the substrate, Figure 2.17(b). The film is bonded to the substrate and the externally applied forces are removed. The substrate will prevent the film from returning to its undeformed state, but the forces from the film will cause the substrate to deform, Figure 2.17(c). Both the film and substrate will bow biaxially and distort near their edges (not shown).

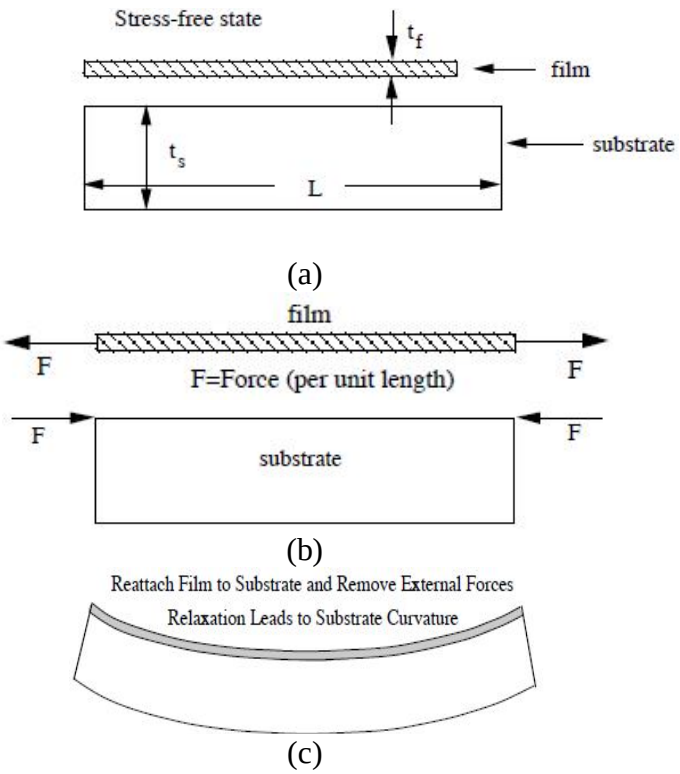


Figure 2.17 The generation of biaxially deformed film-substrate system from, (a) an initially stress-free system. (b) Application of an imaginary external force to the film in order to match the substrate width. The deformed film is attached to the substrate and exerts a stress on the substrate. (c) The biaxially stressed film-substrate system bows in response (Nix 2005).

The stress in the film is assumed to be isotropic and biaxial. Therefore,

$$\sigma_{xx} = \sigma_{zz} = \sigma_f \tag{2.6}$$

where σ_{XX}, σ_{ZZ} and σ_f are the stress tensors in the x-plane, z-plane and biaxial film stress, respectively. The force longitudinally applied to the film is expressed as force per unit length, *F*. Since the cross-sectional area of the film can be thought of in terms of film thickness, t_f, multiplied by length, L, *F* can be expressed as:

$$F = \sigma_f \cdot t_f \tag{2.7}$$

The bending moment, M, generated by *F* applied at the maximum moment arm distance from the neutral axis, $t_s/2$, is expressed by:

$$M = -\sigma_f \cdot t_f \cdot \frac{t_s}{2} \tag{2.8}$$

Substituting this bending moment into the mathematical expression derived from the mechanical analysis of a biaxially deformed plate (see Appendix A) which relates the plate curvature and bending moment, is given by κ:

$$\kappa = -\left(\frac{1-\nu_s}{E_s}\right)\cdot\left(\frac{12\cdot M}{t^3}\right) = -\left(\frac{1-\nu_s}{E_s}\right)\cdot\left(\frac{12\cdot\left(-\sigma_f\cdot t_f\cdot\frac{t_s}{2}\right)}{t^3}\right)$$

$$\kappa = \left(\frac{1-\nu_s}{E_s}\right)\cdot\left(\frac{6\cdot\sigma_f\cdot t_f}{t^2}\right) \tag{2.9}$$

Rearranging equation 2.9, the film stress, σ_f, is:

$$\sigma_f = -\left(\frac{E_s}{(1-\nu_s)}\right)\cdot\left(\frac{t_s^{\,2}}{6\cdot t_f\cdot R}\right) \tag{2.10}$$

This is the well known Stoney Relationship. From this expression, one can measure the curvature of the wafer and extract the stress present in the attached film. Notice that the results only depend on the elastic properties of the substrate and the dimensions of the film and the substrate. It does not depend on the properties of the film. It is important to note that the stress determined by the measurement of the wafer curvature is different than the stress determined from structures fabricated from the film and released from the substrate. Wafer curvature measurements allow for the determination of global constrained stresses, i.e. stress in the wafer before it bends. Micromachined structures that are released from the curved wafers allow for the determination of residual stress, or stresses present after the wafer bending. These residual stresses are attributed to the microstructure, defects, and inhomogeneities present in the film and are therefore much more relevant to films used in MEMS applications.

2.5.3.2 Cantilever Deflection

Beams are the most widely used structural component in MEMS sensors and actuators. They require relatively few processing steps to fabricate and the mechanical principles which govern them are well-defined, which makes the mapping of the measureable data into the final result more dependable. One type of beam structure, the cantilever, is well suited to detect gradient stresses in the film. Gradient stresses are manifested as out-of-plane bends, which can be measured and quantified using beam mechanics. Cantilevers are simple to fabricate and small enough to incorporate onto a device die for the purpose stress management. This section will discuss some basic mechanical properties of a microfabricated cantilever while deriving an expression relating the gradient stress to the curvature of the cantilever.

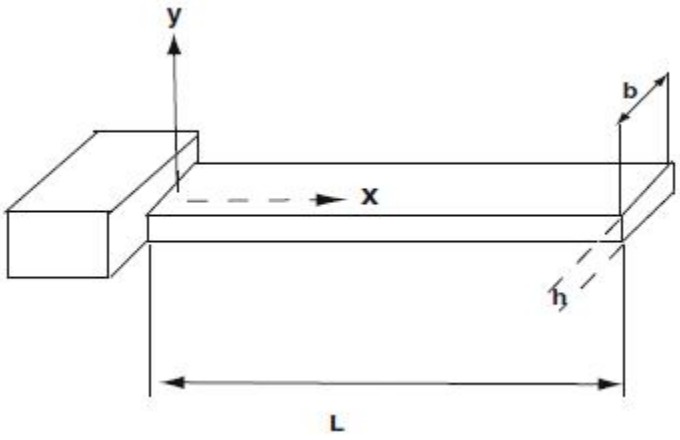


Figure 2.18 Illustration of a cantilever structure with length, "L", width," b", and thickness, "h". The coordinate axis is located so the x-z plane coincides with the neutral plane of the cantilever beam (Nix 2005).

A general residual stress in the plane of a thin film can be envisioned as a superposition of various stress fields represented by the following polynomial series:

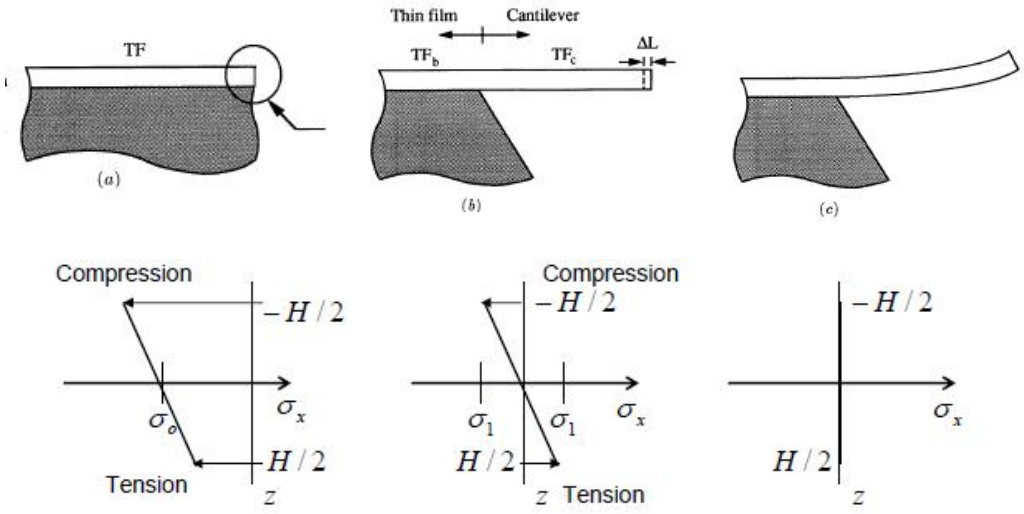
$$\sigma_{total} = \sum_{k=0}^{\infty} \sigma_k \cdot \left(\frac{y}{h/2} \right)^k \tag{2.11}$$

where, h, is the thickness of the cantilever and y is the ordinate of a coordinate system whose x-z plane is located at the neutral plane (midpoint) of the cantilever, see Figure 2.18. The first term of the polynomial, σ_0, is the stress contribution from a uniform, constant stress in the film that is symmetric about the neutral axis. The second term, $\sigma_1(y/(h/2))$, which arises from the gradient stress, is anti-symmetric about the neutral axis and makes a linear contribution to the total stress field, see Figure 2.19. Ignoring the higher terms of the polynomial series, the total stress can be expressed approximately as:

$$\sigma_{total} \approx \sigma_0 + \sigma_1 \cdot \left(\frac{y}{(h/2)} \right) \tag{2.12}$$

When the cantilever structure is released from the substrate, the film-substrate adhesion is removed and the freed structure can deform to relieve its internal stress. The stress field prior to release is shown in Figure 2.19(a). After release, the unrestrained end of the cantilever changes length, ΔL, to relieve the uniform stress, σ_0, and the cantilever curls to relieve the gradient stress, shown in Figure 2.19(b) and (c). This is an idealized scenario in which the higher order terms of equation 2.11 are assumed to be negligible. In fact, the higher order terms may make significant contributions, as may be the case in

heteroepitaxial films or polycrystalline films where the defect concentrations or grain sizes may vary non-linearly through the film.



(a) (b) (c)

Figure 2.19 Stress states present in a thin film cantilever far from the anchor point. (a) The superposition of a uniform constant stress and stress gradient present in the cantilever prior to release from the substrate. (b) After release from the substrate, the constant stress is relaxed via length change of the free-standing cantilever. (c) The stress gradient is relaxed once the cantilever curls out-of-plane. (Fang 1996).

The bending moment present in the cantilever, with width, b, is calculated using the gradient stress term in equation 2.12:

$$M = \int_{-h/2}^{+h/2} b \cdot \sigma \cdot y dy = \int_{-h/2}^{+h/2} b \cdot \sigma_1 \cdot \frac{y}{\left(h/2\right)} \cdot y dy = -\frac{1}{6} \cdot b \cdot h^2 \cdot \sigma_1 \qquad (2.13)$$

The variable, y, is a point between the neutral axis and the edge of the beam along the y-axis, i.e. the moment arm. Using the above bending moment and the area moment

of inertia of a rectangle, $I = (1/12)*b*h^3$, the gradient stress, σ_1 can be expressed as a function of the radius of curvature, R:

$$\kappa = \frac{1}{R} = -\frac{M}{E \cdot I} = -\frac{\left(-\frac{1}{6} \cdot b \cdot h^2 \cdot \sigma_1\right)}{E \cdot \left(\frac{1}{12} \cdot b \cdot h^3\right)}$$

$$\sigma_1 = \frac{E \cdot h}{2 \cdot R} \qquad (2.14)$$

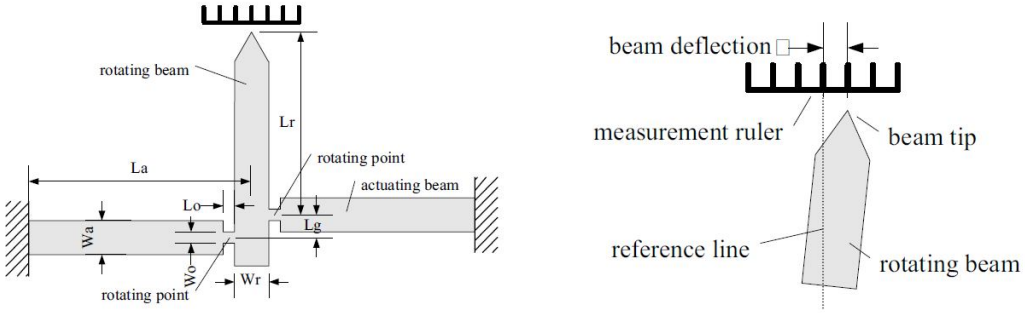
Since the bending is biaxial, $E = E_f/(1-\nu_f)$, where E_f and ν_f are the elastic modulus and the Poisson's ratio of the film, respectively.

2.5.3.3 Planar Rotating Beam

Far-field cantilever bending is primarily due to the presence of a strain gradient (curl). Nevertheless, near the boundary where the cantilever is attached to the substrate, an angular tilt deformation arises from the superposition of the uniform residual stress, σ_0, and from the gradient stress, σ_1. However, the determination of the residual stress through the angular tilt at the boundary reflects the global residual stress, the stress of the SiC- Si heteroepitaxial system. In order to evaluate the local residual stress present in the poly-SiC film, free-standing structures have to be realized.

An effective technique, as reported by Goosen et al., makes use of a micro-rotating structure to measure the local uniform residual stress in the film. The underlying principle of the ability to detect uniform residual stress in the film is by a force couple

generated by two free-standing actuating beam structures on a central, rotating beam, Figure 2.20. When the structure is freed from the substrate, the slightly-offset actuating beams contract (initially, in tension) or elongate (initially, in compression) causing the indicator beam (labeled "rotating beam" in the figure) to deflect. If the beam connections are considered to be ideal, the rotation angle of the indicator (rotating) beam is directly proportional to the strain in the film. A mathematical model can be easily derived using small angle approximations and triangular ratios.



(a) (b)

Figure 2.20 Schematic illustration of a conventional planar micro-rotating structure (Drieenhuizen 1993) used to measure strain gradient in a thin film.

The relationship between tip deflection, y, and the strain is given by:

$$\varepsilon_f = \frac{L_g \cdot y}{(L_A + L_B) \cdot (L_X + (1/2) \cdot L_g)} \tag{2.15}$$

L_g is the distance between the connection of the actuation beams, L_A and L_B, are the lengths of the actuating beams which are designed to be equi-dimensional in most cases. The distance, L_g should be small in order to increase the sensitivity of the sensor,

but not so close that they interact and cause unintentional buckling with films under compressive strain. From the residual strain calculated from equation 2.15, it is possible to determine the residual stress for a biaxial film (equation 2.6) using the stress-strain relationship:

$$\sigma_f = \varepsilon_f \cdot \frac{E}{(1-\upsilon_f)} \tag{2.16}$$

Now that the theoretical basis for both the observed stress in SiC films grown on Si substrates has been presented, along with the means to determine this stress, the next topic involves how the SiC/Si heteroepitaxial films were realized during this dissertation research.

2.6 CVD Reactor Hardware

The CVD reactor used for this research was the horizontal hot-wall reactor shown in Figure 2.24, which was designed and built by the SiC Group at the University of South Florida (Myers 2006). The reactor chamber wall is a fused quartz tube supported by water-cooled electropolished stainless steel endplates. The gases are regulated via mass-flow controllers (MFC) and flow into the head plate (left side of Figure 2.21) by ¼″ 316L stainless steel gas lines. A round diffuser plate consisting of several small, evenly-spaced holes disperses the gas stream and helps to establish laminar flow. The gases are funneled from the diffuser plate by a quartz inlet tube to the hot zone of the reactor. The hot zone consists of a SiC-coated graphite susceptor surrounded by graphite foam

insulating support. The susceptor provides a means of converting electromagnetic energy from the RF induction coils to thermal energy so the necessary CVD reaction can occur at the substrate surface. The ceiling of the susceptor was designed with a gradual taper so that the height of the upstream portion is higher than the downstream portion of the susceptor. The taper causes an increase of the gas velocity as it moves through the susceptor and, as a result, decreases the thickness of the boundary layer. This improves the film uniformity across the wafer. The graphite foam provides a physical means of supporting the susceptor and insulating the susceptor which reduces thermal gradients due to radiative and conductive losses in the susceptor. The water-cooled copper coil surrounding the reactor in Figure 2.21 heats the reactor hot-zone by radio frequency (RF) induction. A 50 kW/ 10 kHz solid state RF generator, manufactured by Mesta Electronics Inc., is capable of inductively heating the susceptor to temperatures greater than 2000°C. The temperature of the hot zone is monitored by an optical pyrometer, which measures temperature by monitoring the susceptor's black body emission. The pyrometer is aimed at a small hole in the susceptor which has been bored to a depth near the growth zone, so that an accurate temperature measurement at the growth zone can be obtained. The temperature and gas flow is regulated by feeding the data back to the RF generator and MFCs, respectively, by a computer interface written in LabView™. The CVD reactor is currently configured to flow propane (C_3H_8) and silane (SiH_4) which serve as the SiC precursor gases, nitrogen (N_2) for n-type doping, and argon (Ar) or hydrogen (H_2) as the carrier or annealing gas. The reactor also has the capability to use hydrogen chloride (HCl) or methyl chloride (CH_3Cl) to add chlorine to the reactor chemistry (Reyes, 2008). The H_2 gas is purified via a palladium cell and the Ar is

purified by a catalytic purifier. An Edwards DP-40 dry pump and throttle valve regulates the CVD chamber pressure.

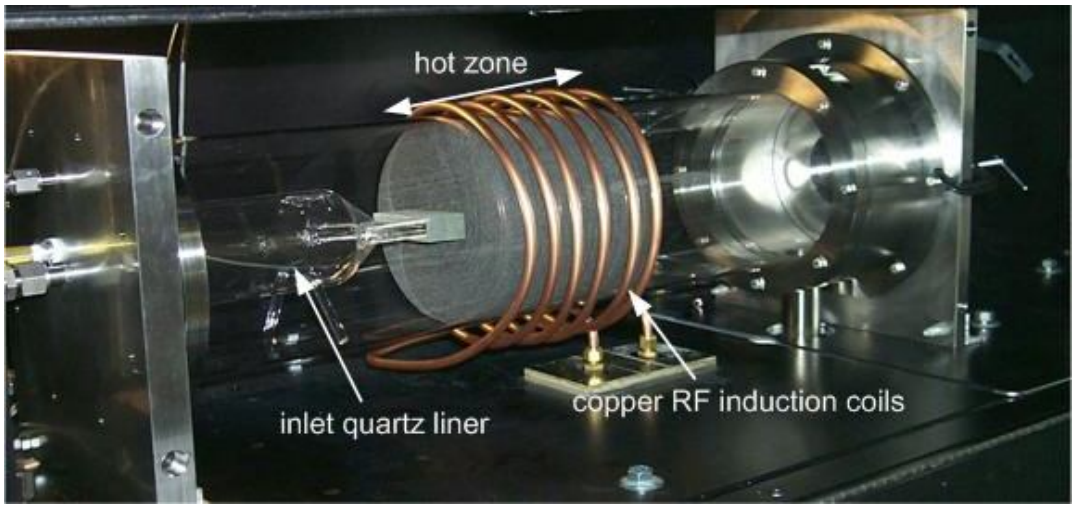


Figure 2.21 Photograph of the MF2 CVD horizontal reactor at USF. MF2 was used for the growth of all films reported in this thesis and is dedicated solely for 3C-SiC on Si growth and processing (Myers 2006).

CHAPTER 3: DEVELOPMENT OF LOW-TEMPERATURE POLY-SiC GROWTH PROCESS FOR POLY-Si-ON-OXIDE SUBSTRATES

Micro-electrical-mechanical systems (MEMS) are used for numerous applications from automobile airbag sensors to combustion control, sensors and medical diagnostics such as DNA assays, just to name a few. These MEMS applications have been supported by Si MEMS, which can be readily made using micromachining techniques developed for the microelectronics industry. One of the powerful fabrication approaches for Si MEMS is the use of poly-Si as the MEMS structure, such as cantilevers and membranes, that are deposited on oxide release layers. These mechanical layers are activated (i.e., released) simply by placing the sample in an HF solution which dissolves the oxide and thus leaves a free-standing poly-Si structure supported over the substrate surface.

One of the drawbacks of Si MEMS is the fact that Si, while a very durable and easy to machine material, is not suitable for harsh environments due to the lack of material resilience at elevated temperatures and when exposed to harsh chemicals and radiation. SiC is a natural material for such harsh-environment sensors, and since SiC can be micromachined using similar processes to Si, much work has been done to develop SiC-based MEMS (Mehregany 1999) (Mehregany 1998). While the cubic form of SiC, 3C-SiC, can be deposited directly on Si and the 3C-SiC layer patterned using reactive ion etching (RIE), the only way to release the 3C-SiC layer is wet KOH etching

of the underlying Si. The resulting material is often rough due to Si residue from the etch which can diminish device performance in addition to adding cost to the device manufacture (KOH etching can take more than an hour in most cases). Being able to employ oxide release layer strategies to SiC-based MEMS clearly would be a major step forward in SiC-MEMS technology, but in order to achieve this goal two things must happen. First, a low temperature 3C-SiC on Si growth process must be developed, which will be discussed in the opening of this chapter. Second, a poly-Si (or single-crystal but very thin) layer must be deposited on top of the oxide release layer to allow for the formation of the 3C-SiC film. In this chapter research to realize exactly these objectives is discussed where we have demonstrated a high-quality poly-3C-SiC on oxide film process that is suitable for subsequent MEMS manufacture which will be the subject of future work as outlined in the following chapter.

3.1 Motivation for Reducing Process Temperature

From an economic viewpoint, the faster growth rate of the high temperature (T > 1300°C) 3C-SiC heteroepitaxial process would make its incorporation into SiC device fabrication desirable. However, the extreme temperatures severely limit the selection of materials during the fabrication to mainly refractory-type materials. Otherwise, device structural integrity may be lost or undesirable diffusion into the surrounding area may lead to device failure. For example, metals such as Au and Al, frequently used in device fabrication, have melting points far below 1380°C and silicon dioxide, having a glass transition temperature near 1200°C, exhibits plastic flow at the temperatures used for high temperature 3C-SiC growth as described in Chapter 2. Another issue arises from the

8% coefficient of thermal expansion (CTE) mismatch between 3C-SiC and Si. When the 3C-SiC hetero-epitaxial film cools from the high growth temperature to ambient room temperature, thermal stress develops at the 3C-SiC/ Si interface putting the 3C-SiC film under tension and inciting stress-relieving mechanisms, such as wafer bow, to emerge. The greater the ΔT between the growth temperature and the cooled 3C-SiC/ Si wafer, the greater the bow. Excessive wafer bow can complicate subsequent processing of the wafer, induce the deformation of free-standing structures, or cause catastrophic substrate fracture or film delamination. Another stress-relieving mechanism is the formation of planar crystal defects such as glide twins and stacking faults.

When these temperature-related issues are considered, the development of a low-temperature ($T \leq 1200°C$) 3C-SiC hetero-epitaxial process appears to be a necessity if 3C-SiC film growth is to be incorporated with other fabrication processes, especially for MEMS applications where oxide release layers are critical.

3.2 Low Temperature Process Development

Since prior 3C-SiC growth on (111)Si had been conducted using a high temperature growth regime (~1380°C), no low-temperature process had been systematically developed. An established low temperature growth process would exploit the morphologically flat films possible on (111) oriented substrates, but with reduced wafer bow and fracturing associated with (111) oriented heteroepitaxial growth. A low temperature growth process would also be compatible for the growth of 3C-SiC on oxide-coated Si compliant substrates.

3.2.1 Low Temperature Baseline Process

The subsequent 3C-SiC growth was performed as follows. A (111)Si wafer was placed in a horizontal, hot-wall reactor heated by the RF induction of a SiC-coated graphite susceptor. The wafer was loaded into a molded poly-SiC plate to fix the position of the wafer within the reactor hot zone. This polyplate was then seated into a recess in the susceptor and the chamber was sealed and evacuated of residual gases. The chamber was then filled with palladium-purified hydrogen to a pressure of 400 Torr. The 3C-SiC process developed for this reactor involves two main process stages, namely the carbonization and growth stages (Reyes 2007). The pressure for the carbonization process was 400 Torr, and growth pressure was 100 Torr based on the high temperature process. The standard gases used for 3C-SiC growth were: palladium-purified hydrogen, H_2, which is used as the transport gas; propane (C_3H_8), which is the carbon precursor; and a 10% silane (SiH_4) premixed in 90% hydrogen ballast(H_2), which is the silicon precursor.

The carbonization stage occurred while the sample temperature was ramped to 1135°C at a rate of ~35 °C/min. Throughout the ramp a flow of 16 sccm of C_3H_8 was maintained with a mass flow controller (MFC), and the H_2 carrier gas flow was maintained at 10 slm. Once the carbonization temperature was reached, the temperature was maintained for 3 min to allow conversion of the (111)Si surface into 3C-SiC. After carbonization and creation of the 3C-SiC template layer, the temperature was ramped a second time at a rate of ~35°C/min to the growth temperature of 1200°C. During this ramp, we determined that it was advantageous to decrease the flow of C_3H_8 while simultaneously introducing and increasing the flow of 10%SiH_4/ 90%H_2 in a step-wise

manner. At the growth temperature the input gas silicon to carbon ratio, Si/C, for the growth stage was 1.2. H_2 flow was maintained at 10 slm until 30°C before the ramp was completed, where it was increased to 40 slm, and the pressure was simultaneously reduced from 400 Torr to 100 Torr. The temperature and gas flows were then held constant, allowing the continued epitaxial growth of 3C-SiC on the carbonized (111)Si wafer. Figure 3.1 graphically summarizes the baseline low temperature process.

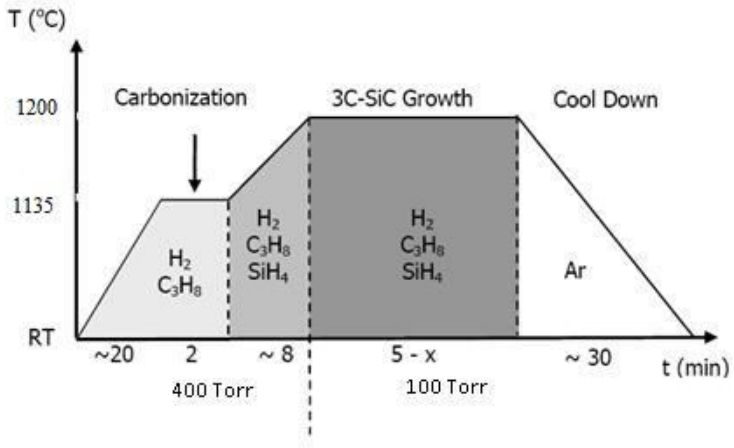


Figure 3.1 Initial baseline low temperature (1200°C) CVD growth process schedule.

The initial test dies yielded a hazy surface over the die that were placed on a standard test polyplate, a sintered SiC plate which holds the 8 x 10 mm silicon dies in a consistent location in the reactor hot zone.

A series of experiments were conducted in order to obtain a uniform, specular film deposition within the growth zone. As briefly discussed in Chapter 2, several parameters govern the film deposition when using chemical vapor deposition. In order to develop an optimized process only one growth parameter was changed at a time while all

others were held constant. Sometimes this can be difficult to achieve if a multitude of experiments are conducted, since the process of film deposition itself alters the reactor condition. The first series of experiments involved decreasing the molar concentration of SiH_4 since it was reasoned that C_3H_8 would not crack as effectively at the lower growth temperature, thus resulting in a Si saturated gas composition. The time of film growth was set at 20 minutes for all experiments since thin polycrystalline films are difficult to discern from thin monocrystalline films in the early stages of growth. In a series of four experiments, the Si/C ratio was varied in increments of 0.2 from 1.4 to 0.8, the C_3H_8 molar concentration was held constant while the 10%SiH_4/ 90%H_2 flux was varied. The best result was obtained for a Si/C ratio of 1.2, although the film was visually hazy in appearance, it demonstrated the least haziness and had the largest grain sizes of the four samples when viewed at 500X magnification using an optical microscope. The next series of experiments involved decreasing the precursor concentration in the H_2 carrier gas. The initial precursor molar fraction values for dilution of 5.5 sccm of C_3H_8 and 200 sccm of 10%SiH_4/ 90%H_2 in 40slm H_2 were $x_{silane}= 0.5x10^{-3}$ and $x_{propane}= 0.139x10^{-3}$. The total precursor concentration was reduced so that the flow rate for propane was 3 sccm. This resulted in molar fractions of $x_{silane}= 0.027x10^{-3}$ and $x_{propane}= 0.075x10^{-3}$. The resulting film morphology was clear and colorful, which indicated very thin film growth. The same experiment was run for 40 minutes to realize a thicker film for a more reliable quality assessment. The resulting 40 minute film growth was hazy and displayed a very granular morphology when viewed using 200X magnification optical microscopy. The SiC deposits on the polyplate revealed an important detail about the deposition pattern occurring in the hot zone of the reactor; it appeared that the optimum deposition was

occurring downstream from the position of the test dies. The H_2 carrier gas flow was then reduced in 5 slm increments from 40 slm to 20 slm while maintaining a constant precursor mole fraction. The best deposition occurred at a 25 slm H_2flow rate. A growth run was performed to assess the deposition rate. A 1 hour growth duration produced a 1.4 μm thick 3C-SiC film. A series of experiments were planned to increase the deposition rate and improve film quality via modification of the Si/C ratio and precursor concentration.

3.2.2 Optimized Low Temperature Process

Once the low temperature baseline process had produced heteroepitaxial films with a clear, specular morphology, the optimum Si/C ratio needed to be determined for the new growth process. Although it was determined that the best morphology occurred at a Si/C=1.2 during the establishment of the low temperature baseline process, the position of the growth zone was moved upstream via carrier gas flow adjustment (reduced flow in this case). As the reactants travel through the hot zone, the Si/C ratio of the gas is constantly shifting in favor of a carbon rich atmosphere. This is believed to be the result of the Si supplied by SiH_4 being unavailable for surface reactions due to the formation of Si clusters in the gas stream (Vorob'ev, et al. 2000). Again, a series of film growths were conducted by varying only the Si/C ratio in 0.1 increments ranging from 1.2 to 0.9 while all other growth parameters were held constant. The samples were visually inspected under an optical microscope and it was determined that a Si/C=1.1 displayed the smoothest surface morphology with the fewest inclusions. Although visual inspection of the film provides only a qualitative assessment of film quality, surface

morphology is frequently related to crystal defects and this approach is a valuable tool when simplicity and immediate feedback is required.

An increase in the deposition rate was the focus on the next set of experiments. The current growth schedule involved diluting 3 sccm of C_3H_8 and 99 sccm of 10%SiH_4/ 90% H_2 in 25 slm of H_2 carrier gas while under 100 Torr of pressure at 1200° C. The precursor concentration was increased to $x_{propane}= 0.16x10^{-3}$ and $x_{silane}= C_3H_8= 4$ sccm and 10%SiH_4/ 90%H_2=120 sccm diluted in 25 slm of H_2, maintaining the Si/C ratio at 1.1. The flow rate of C_3H_8 and 10% SiH_4/ 90% H_2 was increased to 4.0 sccm and 120 sccm, respectively. The resulting film was hazy and exhibited a granular morphology under optical microscope inspection. A growth run using a flow rate of C_3H_8=3.5 sccm and SiH_4= 115 sccm also demonstrated degraded film quality. The process pressure was further reduced from 100 to 75 Torr, the lowest obtainable pressure for the low temperature growth condition in the MF2 reactor. The pressure was decreased in an attempt to increase the amount of available reacting Si species by decreasing the tendency to form Si clusters. Computer modeling and experiments suggest that the deposition rate is sensitive to the available Si bonding sites (Vorob'ev, et al. 2000). By decreasing the pressure, Si clusters should tend to dissociate, maintaining all other variables unchanged from the 100 Torr growth schedule. The resulting film grown at 3 sccm of C_3H_8, 99 sccm of 10%SiH_4/ 90% H_2 diluted in 25 slm H_2carrier gas under 75 Torr yielded improved film morphology. Unfortunately attempts to increase the precursor molar concentration resulted in degraded film morphology.

A growth run on an RCA cleaned, quartered 50 mm (111) Si wafer was performed to assess the film deposition rate. A forty-five minute 3C-SiC deposition

experiment was conducted and measurements via FTIR yielded a growth rate that increased from 1.4 μm/h to 1.9 μm/h. The process conditions resulted in a clear, specular film. The film morphology was assessed using optical microscopy and atomic force microscopy. However, the bowed substrate revealed the presence of residual film stress. No fractures could be seen visually with the unaided eye, but under 200X, small cracks could be seen. A subsequent growth experiment was performed on an RCA cleaned, 50 mm (111)Si wafer using the optimized low temperature/ low pressure growth process. The duration of the growth plateau was 90 minutes and yielded a 2.84 μm thick film (measured at the wafer center). The wafer was noticeably bowed and fractures could be seen with the unaided eye across the wafer surface. The cracks formed a triangular pattern along the <110> directions on the wafer.

The low-temperature (111)3C-SiC process was then applied at increased growth temperatures up to 1380°C. The plot of the natural logarithm of the growth rate versus the inverse of the deposition temperature is illustrated in Figure 3.2. The low negative slope suggests a transport-limited regime for the 75 Torr low temperature growth process. This was expected since a previous experiment showed that the growth rate decreased from 4.5 μm/h to 3.2 μm/h when the pressure was increased from 100 Torr to 400 Torr at 1380°C.

Atomic force microscopy (AFM) scans were performed to ascertain the surface morphology of the 3C-SiC films. X-ray diffractometery (XRD) was performed on the 3C-SiC film to verify the film orientation and crystalline quality.

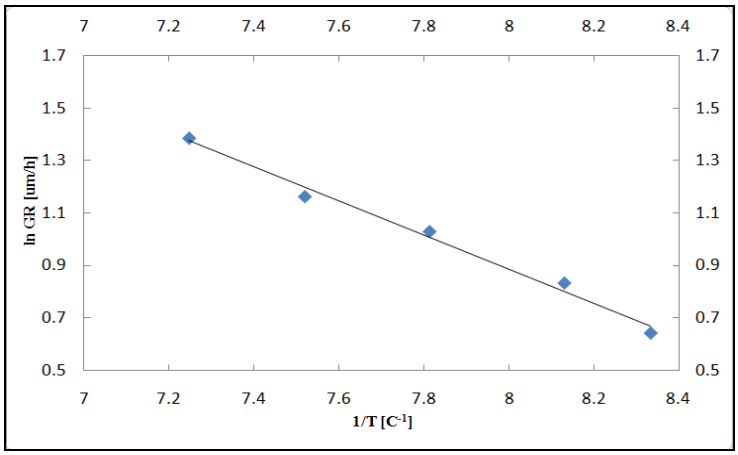


Figure 3.2 Plot of the deposition rate vs. inverse temperature using the optimized low-temperature/ low pressure growth process at various growth temperatures.

3.3 Poly-SiC Growth on Poly-Si-on-Oxide Substrates

The growth of polycrystalline SiC, grown on a poly-Si seed layer previously deposited on an oxide release layer (see chapter 2) was studied next. Highly oriented 3C-SiC films were formed directly on an oxide release layer, composed of a 20-nm-thick poly-Si seed layer and a 550-nm-thick thermally deposited oxide on a (111)Si substrate, was investigated as an alternative to using SOI substrates for freestanding SiC films for MEMS applications. The resulting SiC film was characterized by x-ray diffraction (XRD) with the x-ray rocking curve of the (111) diffraction peak displaying a FWHM of 0.115º (414″), which was better than that for 3C-SiC films grown directly on (111)Si during the same deposition process. However, the XRD peak amplitude for the 3C-SiC film on the poly-Si seed layer was much less than that for the (111)Si control substrate due to slight in-plane misorientations in the film. Surprisingly, the film was solely composed of (111)3C-SiC grains and possessed no 3C-SiC grains oriented along the <311> and <110> directions which were the original directions of the poly-Si seed

layer. With this new process, MEMS structures such as cantilevers and membranes can be easily released leaving behind high-quality 3C-SiC structures.

3.3.1 Motivation for 3C-SiC Growth on Oxide Layers

SiC is a semiconductor material that is desirable for many power electronics and MEMS applications due to its wide band gap, mechanical resilience, robust thermal properties, and chemical inertness. However, many of these inherent properties create extreme difficulties when processing MEMS devices with this material. SiC chemical resistance reduces the effectiveness of wet chemical etching and requires the use of dry etching techniques involving reactive ion etching (i.e., DRIE/RIE). Fortunately, cubic silicon carbide, 3C-SiC, is the one polytype of SiC that can be grown heteroepitaxially on Si substrates, and the addition of this Si layer allows for many more processing options in device manufacturing. For example, one can utilize the Si substrate as a sacrificial layer for the creation of freestanding 3C-SiC MEMS structures (Beheim and Evans 2006) (Carter, et al. 2000). However, the recipes used to etch Si in DRIE/RIE have a similar etch rate with SiC, thereby excluding selectivity and reducing accuracy for the desired structure (Beheim and Evans 2006) (McLane and Flemish 1996) (Rosli, Aziz and Hamid 2006). Freestanding SiC MEMS devices using sacrificial Si layers have also encountered difficulties during device fabrication resulting from unetched Si preventing the complete release of the structure (Beheim and Evans 2006) (Carter, et al. 2000). Silicon dioxide, SiO_2, has been traditionally used as an etch-stop in Si processing involving DRIE/RIE, and can be easily removed by wet chemistry processes to allow for the full release of freestanding structures (Federico, et al. 2003). With this in mind, silicon-on-insulator,

SOI, substrates provide an excellent media for the creation of freestanding SiC devices by providing not only an oxide for the etch-stop for DRIE/RIE, but also a Si crystal seed layer for the heteroepitaxial growth of the 3C-SiC (Shimizu, Ishikawa and Shibata 2000) (Myers, Saddow, et al. 2004).

SOI provides some additional benefits for the growth of 3C-SiC as shown in previous studies (Shimizu, Ishikawa and Shibata 2000) (Myers, Saddow, et al. 2004). The high temperatures required for the growth of single-crystal 3C-SiC soften the SiO_2 layer, allow dispersion of stress caused by the ~20% lattice mismatch between SiC and Si, and suppress the formation of voids caused by Si evaporation at the 3C-SiC/ Si interface (Carter, et al. 2000). Although thick SOI seed layers (>50 nm) have been shown to produce 3C-SiC films that are of comparable quality when compared to 3C-SiC films grown on single-crystal Si substrates, the benefits of the epitaxial growth of 3C-SiC on SOI are only realized when 3C-SiC is deposited on a thin (<50 nm) seed layer of Si, which produces excellent quality 3C-SiC (Shimizu, Ishikawa and Shibata 2000) (Myers, Saddow, et al. 2004). However, a major drawback of using SOI in the production of 3C-SiC devices is the fact that it requires extensive processing techniques (Shimizu, Ishikawa and Shibata 2000) (Myers, Saddow, et al. 2004). These processes add to the overall production cost of the device. In addition many MEMS devices do not require single-crystal SiC material for proper functionality. A cost-efficient, easily produced wafer stack consisting of poly-Si/ SiO_2/ Si layers could replace the SOI substrate if poly-SiC is desired as a material for MEMS applications.

3.3.2 Deposition of Poly-Si Layer on SiO_2/ (111)Si

For our experiments we replaced the expensive SOI wafer with a stack of poly-Si/ SiO_2/ (111)Si, where the poly-Si serves as the seed layer for the subsequent growth of poly-SiC. The results of the growth were surprising because, instead of producing a layer of typical poly-SiC, the resulting growth was 3C-SiC that was highly oriented in the <111> direction, and contained no grains in the <110> direction, which was the favored orientation of the poly-Si grains. Substrate preparation for the growth experiments was as follows. A (111)Si wafer was RCA cleaned, followed by the CVD deposition of 5500 Å of silicon dioxide. After oxidation, a 50-nm-thick film of poly-Si was deposited by LPCVD at a temperature of 610°C and a pressure of 300 mTorr (Harbeke, et al. 1984). This process was chosen from the various poly-Si recipes for many reasons. The first is that a compressive stress is produced between the resulting poly-Si film and the oxide layer, which should help bring the Si crystal lattice into greater compliance with the 3C-SiC crystal lattice (Yang, et al. 2000). A secondary reason for the growth of poly-Si at this temperature is that it generates large columnar Si grains textured mainly in the <110> direction with a minor presence of grains textured in the <111> and <311> directions (Harbeke, et al. 1984). The resulting thin poly-Si film was characterized by both AFM and XRD to ascertain the starting growth surface properties. The AFM, performed on a PSIA XE-100 microscope, shows a surface with grains of average area on the order of 5.5 nm^2, having an average surface roughness of 0.49 nm rms, but also indicated the presence of pinholes in the surface. The XRD measurements were performed on a Philips Panalytical X'pert Diffractometer operating at the Cu K-α line, and the measurements indicated alignment of the poly-Si grains in the <110>, <111>, and <311>

directions, as was expected from the literature (Harbeke, et al. 1984) (Yang, et al. 2000). The pinholes created difficulties during the deposition of 3C-SiC by creating a pathway for softened oxide material to flow onto the growth surface thus damaging the 3C-SiC film morphology. Therefore, as outlined in the last section, the temperature for growth was reduced from the temperatures developed previously (M. Reyes, et al.) to eliminate this problem, resulting in the maximum growth temperature for 3C-SiC on the film stack of 1200°C.

3.3.3 Polysilicon Carbide Growth Process

The final optimized growth process is as follows. The poly-Si/ SiO_2/ (111)Si wafer stack was placed in a horizontal, hot-wall reactor heated by the RF induction of a SiC-coated graphite susceptor as outlined in Chapter 2. The wafer was loaded into a molded poly-SiC plate to fix the position of the wafer within the reactor hot zone. This poly-SiC plate was then seated into a recess in the susceptor and the chamber was sealed and evacuated of residual gases. The chamber was then filled with palladium-purified hydrogen to a pressure of 400 Torr. The 3C-SiC process developed for this reactor involves two main process stages, namely the carbonization and growth stages (Reyes 2006). The pressure for the carbonization process was 400 Torr, and growth pressure was 100 Torr. The standard gases used for 3C-SiC growth are: palladium-purified hydrogen, H_2, which is used as the transport gas; propane (C_3H_8), which is the carbon precursor; and a 10% silane (SiH_4) premixed in hydrogen, which is the silicon precursor.

The carbonization stage occurred while the sample temperature was ramped to 1135°C at a rate of ~ 35°C/min. Throughout the ramp, a 2.38×10^{-3} C mole fraction was

maintained. Once the carbonization temperature was reached, the temperature was maintained for 3 min to allow for conversion of the poly-Si surface into 3C-SiC. After carbonization and the creation of the 3C-SiC template layer, the temperature was ramped a second time at a rate of ~35°C/min to the growth temperature of 1200°C. During this ramp, we determined that it is advantageous to slowly decrease the flow of C_3H_8 while simultaneously introducing and increasing the flow of SiH_4. H_2 flow was maintained at 10 slm until 30°C before the ramp was completed, where it was increased to 25 slm, and the pressure was reduced from 400 Torr to 100 Torr. At the growth temperature the silicon to carbon ratio, Si/C, for the growth stage was 0.94, with a 3.94×10^{-4} C mole fraction and a 3.71×10^{-4} Si mole fraction. The temperature and gas flow were then held constant, allowing for the continued epitaxial growth of 3C-SiC on the carbonized poly-Si buffer layer. The reactor had no wafer rotation, so the process parameters produced a growth rate of 3.0µm/h near the upstream-side of the wafer and 2.5µm/h at the downstream-side of the wafer due to precursor depletion. This rate, measured using an Accent QS-1200 FTIR system to determine film thickness, was also verified on samples of 3C-SiC grown on single-crystal Si oriented in the <100> and <111> directions using identical process conditions as reported above.

3.4 Analysis of the Poly-SiC-on-Oxide Film

3.4.1 AFM Analysis

Atomic Force Microscopy (AFM) surface analysis was used to characterize the film morphology as shown in Figure 3.3. The growth of SiC on the poly-Si/ SiO_2/ (111)Si substrate was compared with 3C-SiC grown directly on (100) and (111)Si substrates. The morphology of the surface of the 3C-SiC on the poly-Si stack was similar to that of the 3C-SiC grown on Si (111), showing growth of ordered triangular island grains of similar size. The AFM micrograph of 3C-SiC grown on Si (100) has smaller, rounded, and more disassociated island growth with a large distribution in grain size. A cross-section SEM micrograph displays the growth of 3C-SiC on the poly-Si stack near the downstream sector of the wafer shown in Figure 3.4. This cross-section SEM, performed on a Hitachi 4800 microscope, shows that the thickness of the 3C-SiC film grown for 30 min on the poly-Si stack was ~1.3 μm, verifying the growth rate as measured by FTIR. An important aspect of this growth process is that the oxide remained perfectly intact and was unaffected during the growth of the 3C-SiC.

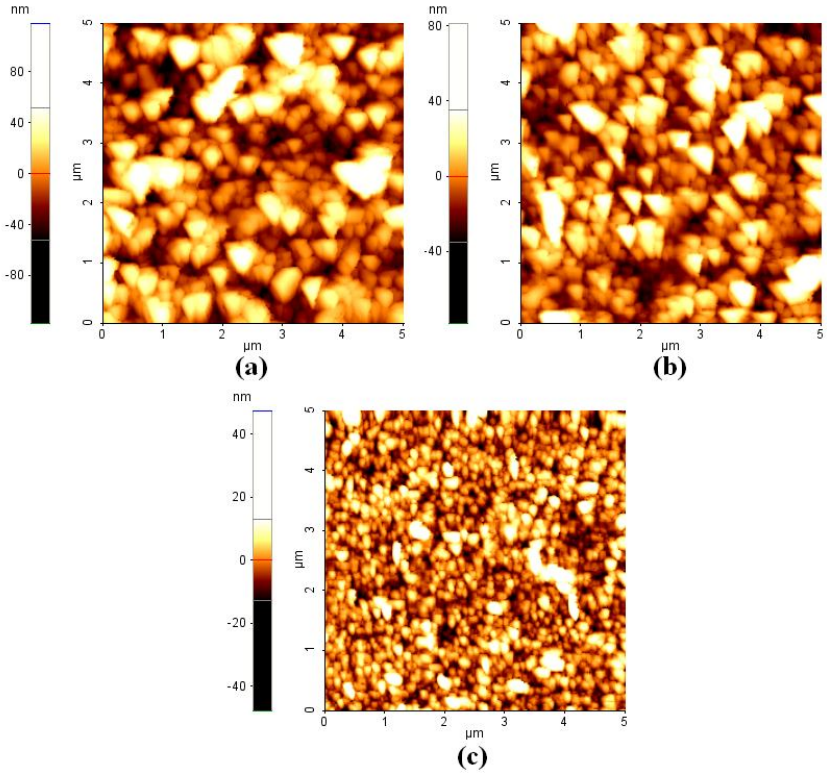


Figure 3.3 AFM micrographs of the surfaces of the SiC deposition grown on (a) poly-Si/ SiO_2/ (111)Si, (b) (111)Si, and (c) (100)Si. The 5µm x 5µm images were collected in contact mode using a SiN tip. The respective z resolution and r_q values are (a)-78nm to 81.4nm, r_q=17.9nm, (b) -117.3nm to 118.4nm, r_q= 26.5nm, and (c) -47.7nm to 47.5nm, r_q=6.57nm.

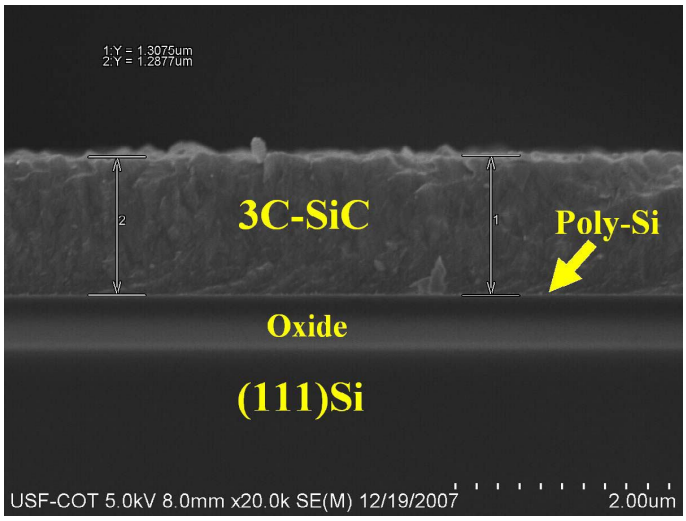


Figure 3.4 Cross-section SEM micrograph of a 3C-SiC film grown on the poly-Si/ SiO_2/ (111)Si compliant stack. The 3C-SiC grown has a thickness of ~1.3µm and the SiO_2 layer is ~0.55µm thick. The poly-Si layer was estimated to be ~20nm. Note that the SiC/ SiO_2 interface is undamaged. SEM analysis conducted by D. Evans, SRI, Largo, FL.

3.4.2 XRD Analysis

Figure 3.5 shows the θ-2θ x-ray diffraction (XRD) spectra and high-resolution rocking curves performed on the 3C-SiC films for determination of the crystal orientation and quality of the 3C-SiC layer. For the 3C-SiC film grown on the poly-Si/ SiO_2/ (111)Si stack a very strong peak was observed at 35.6º while a weaker peak at ~71.8º is due to reflections from the (111)3C-SiC and (311)3C-SiC planes, respectively. It is also evident that there are no SiC reflections originating from the <110> direction, which were the main grain orientations present in the poly-Si seed layer. A comparison of the relative peak intensities suggests a preference for grain alignment in the <111> direction, while very few grains appear to be aligned along the <311> direction. The 3C-SiC films grown on (111)Si and (100)Si show dominant peaks at 35.6° and 41.4°, respectively.

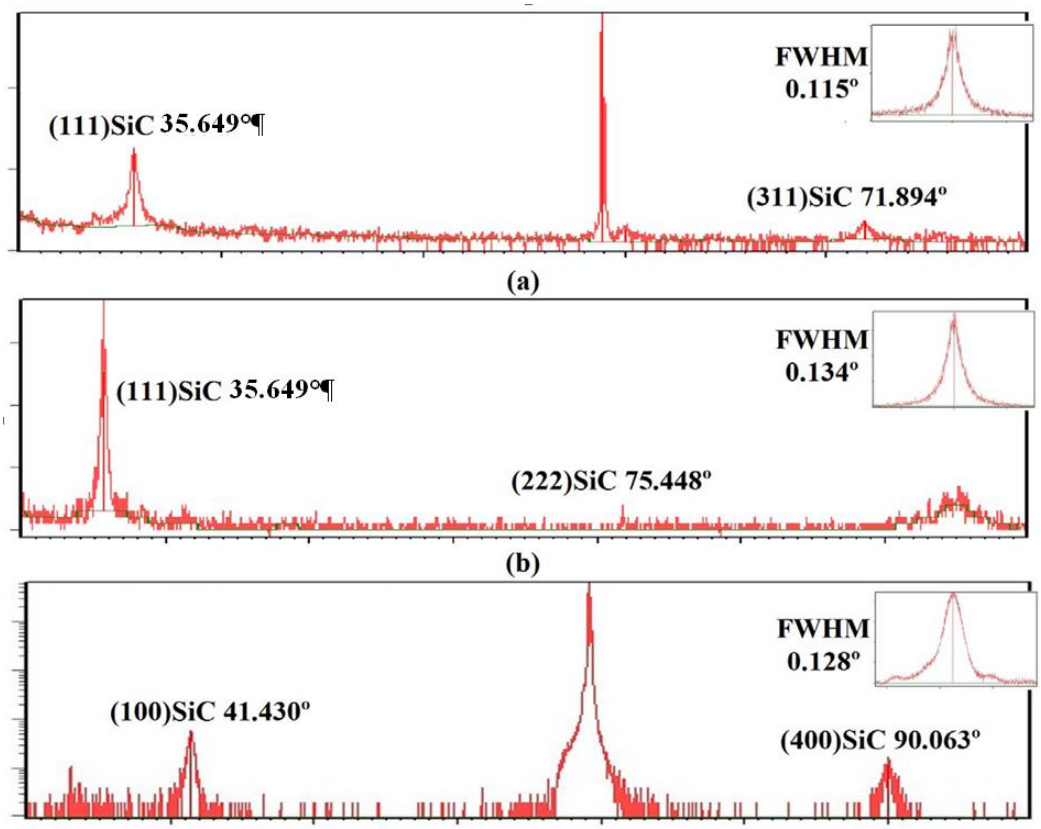


Figure 3.5 XRD θ-2θ diffraction surveys for the 3C-SiC films grown on (a) poly-Si/ SiO_2/ (111)Si, (b) (111)Si, and (c) (100)Si substrates. The XRD θ-2θ scans show that (a) and (b) possess a primary peak at 35.6°, and (c) possesses a primary peak at 41.4°. Insets: rocking curves for each of the 3C-SiC films taken at their respective primary Bragg peaks. The FWHM values are 0.115° (414″), 0.134° (482″), and 0.128° (460″), respectively.

The rocking curves were taken at the primary Bragg peak for each the 3C-SiC epitaxial films. The insets displayed in Figure 3.5 show the results of the rocking curves obtained for each substrate type. The rocking curve for the 3C-SiC films on poly-Si/ SiO_2/ (111)Si substrate displayed a FWHM of 0.115º (414″), the 3C-SiC on (111)Si was 0.134º (482″), and the 3C-SiC on (100)Si displayed FWHM value of the 41.4° peak of 0.128º (460″). The correlation of the FWHM values from the growth performed on poly-Si/ SiO_2 / (111)Si versus the growth performed on single-crystal Si appears to suggest

that all films have relatively comparable crystallinity. This correlation proves to be very interesting because the growth of the 3C-SiC film on the poly-Si/ SiO_2 / (111)Si stack began on a poly-Si seed layer with multiple orientations, and when compared to 3C-SiC films by Carter, et al. (Carter 2000) grown on SOI of similar Si seed and oxide layer thicknesses (50 nm and 0.5 μm, respectively), the reported FWHM value was 0.20° (720″), which is almost double the FWHM of the 3C-SiC grown on the poly-Si seed reported in this work.

Speculation suggests that the result of the weak amplitude from the Bragg reflections seen in the θ-2θ diffraction scan and the relatively narrow FWHM measurement from the rocking curves indicate a highly-ordered polycrystalline 3C-SiC layer in which the crystallites are misaligned relative to each other but all appear to be of the <111> direction. While the <111> direction of the 3C-SiC planes of the various grains are still approximately parallel to one another, producing a relatively narrow rocking curve, the (111) planes rotated about the <111> direction would produce a weak amplitude count in the θ-2θ survey.

3.5 Summary

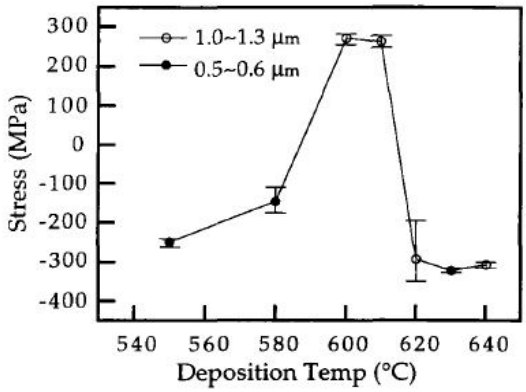
In summary, a well ordered polycrystalline 3C-SiC film with grains predominantly along the <111> direction has been successfully grown on a poly-Si/SiO_2/ (111)Si wafer and the process results verified multiple times. This process was developed to create an easy to release 3C-SiC layer for use in MEMS applications and, therefore, will be useful for MEMS applications that will benefit from 3C-SiC structures. The cost-effectiveness and relative ease for the deposition of both oxide and poly-Si make this

process superior to the methods used to fabricate SOI substrates, and the oxide layer provides more device processing options than 3C-SiC grown directly on single crystal Si. Fortuitously, the resulting 3C-SiC films were highly ordered in the <111> direction and their quality assessed using AFM, SEM, and XRD analysis. The quality of the ordered 3C-SiC grown on the poly-Si stack is comparable to that of 3C-SiC grown on a single crystal Si, and much better than that of 3C-SiC grown on conventional SOI as reported in literature.

CHAPTER 4: INFLUENCE OF POLYSILICON SEED-LAYER THICKNESS ON POLY-SiC RESIDUAL STRESS

In Chapter 2, it was briefly discussed that the intrinsic stress present in thin films was determined by many non-equilibrium growth processes that take place early during the film's deposition. The grain structure, size and growth evolution are the manifestations of the cumulative effect of these processes and, as a result, they play a vital role in stress management. The use of a polysilicon seed-layer to grow poly-SiC can have the advantage as serving as a template to influence the grain growth evolution in the poly-SiC film in a way that is analogous to using a carbonization plateau to reduce defects in crystalline 3C-SiC. Polysilicon can exhibit intrinsic compressive or tensile stress depending on the deposition conditions, most notably the deposition temperature, Figure 4.1 (Harbeke, et al. 1984). Compressive polysilicon films are attractive candidates as a seed layer for poly-SiC films since the compressed grains should have a slightly reduced lattice parameter which would help reduce the lattice mismatch between Si and 3C-SiC. The nature of this compressive stress is not entirely understood, but it has been postulated to be a result of hydrogen incorporation (Yu 1997), the diffusion of excessive adatoms into the grain boundaries, or grain crowding due to lateral grain growth (X.-A. J. Fu 2004) (Maier-Schneider 1996). Polysilicon films grown at deposition temperatures $\geq 620°C$ exhibit colmunar grain structure (Harbeke, et al. 1984) (Maier-Schneider 1996)

that evolves in a conical fashion, i.e. the grain size projected on the surface increases as the film thickness increases. Thicker polysilicon films should have larger and highly-textured grain faces on which poly-SiC growth can begin. This should lead to large columns of highly-textured poly-SiC crystallites exhibiting lower uniform intrinsic stress and reduced stess gradients.



T_d (°C)	D_{111} (Å)	D_{220} (Å)	D_{311} (Å)	Texture
As-grown				
560	X-ray amorphous			—
570	X-ray amorphous			—
580	770	290	240	Weak <311>
600	110	340	180	<311>
620	140	770	180	<110>

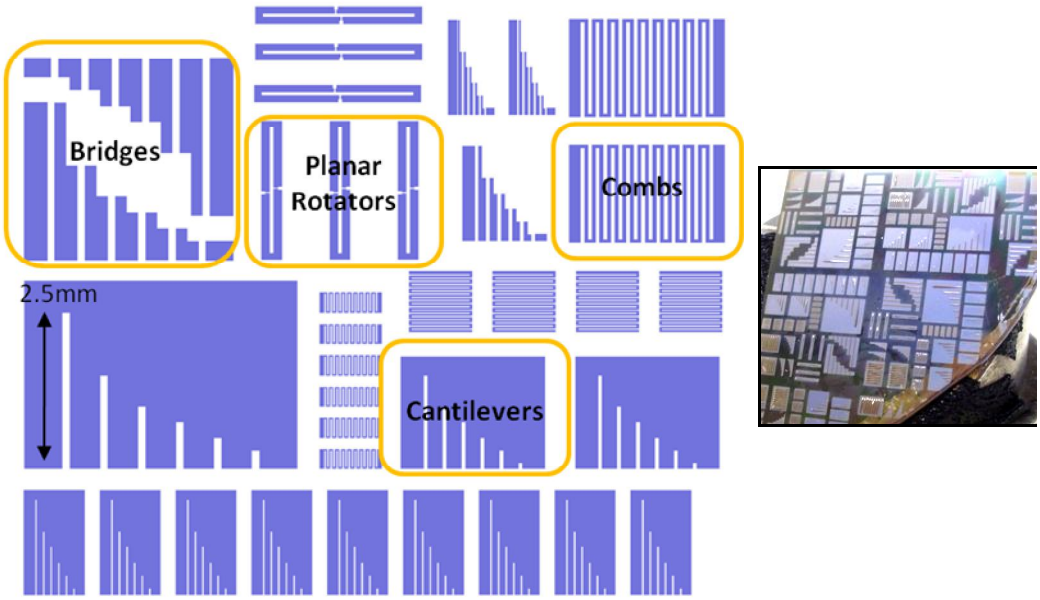
Figure 4.1 Stress as a function of deposition temperature for polysilicon films. Note that the films deposited at < 580°C are compressive and amorphous, while the films deposited at ≥620°C are compressive and polycrystalline (Yu 1997).

Chapter 3 discussed the establishment of a low-temperature growth process based on the vitrification temperature of PECVD oxide (Polian 2002) and the preferential grain growth in the <111> direction of the poly-SiC film grown on polysilicon-on-oxide substates. The low-temperature process described in Chapter 3 was developed using unpatterned polysilicon-on-oxide substrates. The realization of poly-SiC MEMS

structures using polysilicon-on-oxide substrates would mean that the oxide layer would have to be patterned and then coated with a thin polysilicon film. CVD-grown poly-SiC is deposited on the substrate and then micromachined using standard Si-based processing techniques. The opening of Chapter 4 will describe the details of the fabrication process following afterwards with a description of the methods used to characterize the structures. Chapter 4 will conclude with a discussion of the results.

4.1 Fabrication of SiC MEMS on an Oxide Release Layer

An acetate test mask was designed using fundamental beam structures of varying dimensions such as cantilevers, double-clamped beams (bridges), and planar rotating structures, shown in Figure 4.2. This mask set served as a test-bed to find the optimum dimensions to use for stress-strain sensitive microstructures fabricated from poly-SiC grown on polysilicon-on-oxide substrates. Due to the limitations of the printing emulsion used to print on the acetate, the feature resolution was limited to 20 μm. However, the low cost and rapid production time made the acetate masks a good choice for design trials. The acetate mask was attached to 5" x 5" soda-lime glass squares using double-sided cellophane tape to serve as a rigid frame to stabilize the mask during photolithography.



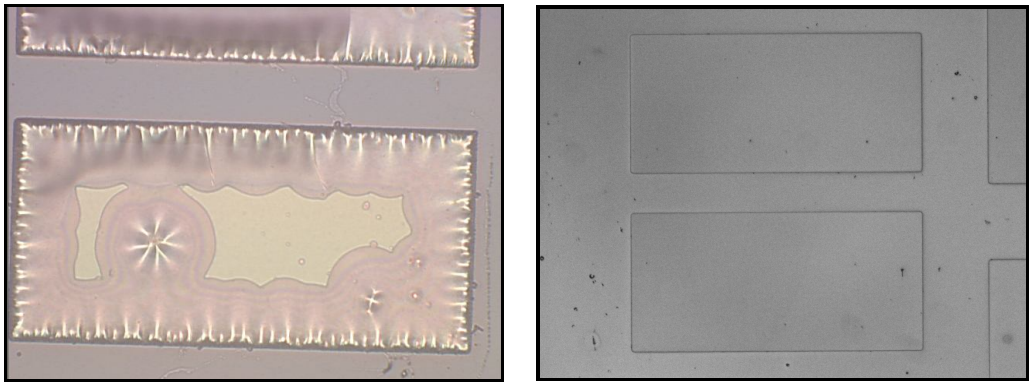
(a) (b)

Figure 4.2 (a) Mask layout details of the first test mask consisting of cantilevers/ combs, bridges, and planar rotators of various dimensions. (b) ¼ wafer of 3C-SiC on Si processed with this mask.

4.1.1 Test Growth on Patterned Polysilicon-on-Oxide Substrates

A test process was performed on an unpatterned, previously-fabricated monocrystalline, 2 inch (111)Si wafer containing a PECVD-deposited a 1µm thick oxide layer coated with a 90 nm thick LPCVD polysilicon layer. It was unclear how well a patterned oxide would endure during the low-temperature growth process, since all previous growth was done on fully-intact substrates. The polysilicon-on-oxide wafer was patterned with AZ® 4620, a robust photoresist used in plasma etching, and dry etched to remove unwanted material (described in more detail below). Poly-SiC was then grown on the mesa-like poly-Si/ oxide patterns (Figure 4.3) using the low-temperature process described in Chapter 3.

Visual inspection of the wafer revealed that delamination of the 3C-SiC film had occurred. Closer inspection of the film via optical microscopy showed evidence of film buckling and glass flow of the underlying oxide layer through pinholes in the polysilicon seed-layer (see Figure 4.3(a)). The delamination could have been caused by the discontinuous transition from a monocrystalline film (grown in windows in the oxide/polysilicon films) to a polysilicon film (grown on the mesas), or the oxide layer softening too much and loosing traction with the poly-SiC during growth. To correct this problem, the polysilicon seed-layer was stripped from the remaining poly-Si-on-oxide substrates so that a thin conformal layer of polysilicon could be uniformly deposited after the oxide was patterned for the anchor points. It was decided to grow the 3C-SiC at 1150 °C, which should be below the expected ~1200 °C glass-transition temperature of the oxide to prevent viscous flow, but hot enough to allow the compliant benefits of the softened oxide layer. The results are shown in Figure 4.3(b)



(a) (b)

Figure 4.3 Optical micrographs of 3C-SiC grown on the patterned poly-Si/ SiO_2/ (111)Si substrates. (a) 3C-SiC grown at 1225 °C from polysilicon only present on the oxide mesas (light colored regions). (b) 3C-SiC grown at 1150 °C from uniform, conformal polysilicon deposited over the entire substrate. Note the absence of film buckling at the edge of the oxide mesas and glass flow through pinholes in the polysilicon layer.

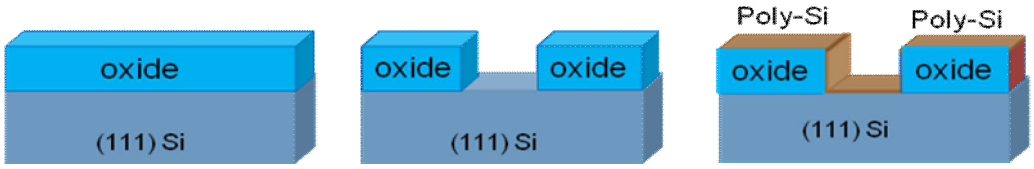
4.1.2 Poly-SiC MEMS Fabrication Procedure

RCA-cleaned (Kern and Poutinen 1970), 2 inch diameter, (111)-oriented Si wafers were PECVD-deposited with a 1.5µm thick layer of oxide. The oxide-coated (111)Si wafers were then spin coated at 2200 rpm for 2 minutes using AZ® 4620, a positive photoresist used as a dry etch mask, to achieve a thickness of 7µm. The photoresist-coated wafer was then soft-baked for 1 min at 115 °C on a hotplate followed by a 20 min cooldown. The photoresist was aligned and patterned with the anchor trenches using a Quintel Mask Aligner. The exposure time was 22 seconds using a filtered UV source with a light intensity of 19 mW/cm^2 optimized at g-line emission. The exposed wafer was then developed using AZ® 400K, a developer suited for use with AZ® 4620, diluted 1:4 with deionized water. The patterned wafer was then rinsed with deionized water, dried with dry N_2 and examined.

Etching of the wafer was carried out using an Alcatel AM-100 Deep Reactive Ion Etcher (DRIE). The plasma etching chemistry utilized a gas mixture of octafluorocyclobutane, C_4F_8, and methane, CH_4, excited by a 2500 W RF source. The etch rate of the oxide was ~300 nm/min. The residual photoresist mask was cleaned with acetone-followed by a methanol rinse.

The patterned-oxide wafers were then RCA cleaned prior to their loading in a LPCVD furnace for polysilicon deposition. The deposition temperature was held at 610 °C under 250 mTorr pressure while 100 sccm of SiH_4 flowed. Previous measurements of thicker film depositions made using this recipe indicated that 1 min of actual deposition time was necessary to deposit ~20nm of polysilicon. The estimated film thickness was confirmed via ellipsometry. A second set of wafers were deposited with polysilicon

using the same recipe with a 8 min deposition time. Figure 4.4 illustrates a brief summary of the process.



(a) (b) (c)

Figure 4.4 Summary of the patterning of anchor points for the SiC-based MEMS structures prior to epitaxial growth of the 3C-SiC. (a) An oxide layer is PECVD deposited on a (111)Si substrate. (b) Windows for anchor points are etched into the oxide layer. (c) A 50-100 nm thick polysilicon layer, serving as a seed-layer for 3C-SiC growth, is LPCVD deposited on the patterned oxide.

The patterned poly-Si-on-oxide stack was then diced into quarters and loaded into a horizontal hotwall SiC CVD reactor (Figure 4.5). It was also decided to incorporate a control sample consisting of a patterned monocrystalline (111)Si quarter wafer deposited with the polysilicon seed-layer to compare against the polysilicon-on-oxide substrate. The low temperature growth process is outlined in Chapter 3, section 3.2.2, was then employed to grow a 0.5 um thick poly-SiC film. The reactor was then passively cooled under constant Ar purge to ambient room temperature and extracted for detailed characterization.

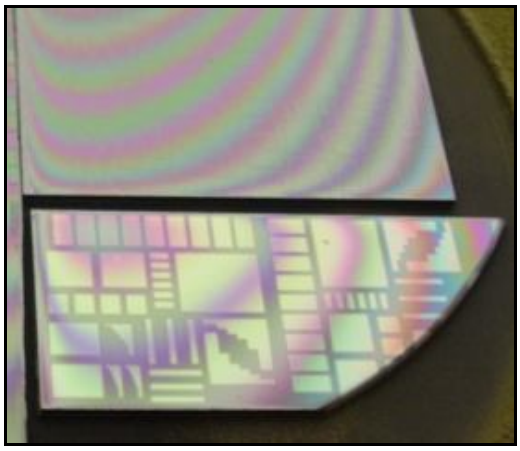


Figure 4.5 A polysilicon-on-oxide substrate after poly-SiC deposition. The anchor points for the structures are the "streets" between the lighter-colored polysilicon/ oxide "mesas". The control sample (patterned (111)Si) is also shown for reference (top).

Both samples were again spin-coated at 2200 rpm with AZ® 4620 then aligned and patterned with the MEMS structure mask. The exposed 3C-SiC was DRIE etched using an SF_6/O_2 chemistry under DC bias, Figure 4.6. The attempt to release the MEMS structures using an HF vapor etch immediately revealed problems with surface-tension stiction and suggested that a thicker oxide layer should be implemented in future polysilicon-on-oxide substrates to facilitate structure release. The (111)Si substrate exposed after removal of the oxide was etched using a 1:20 NH_4F: HNO_3 solution to allow enough clearance between the MEMS devices and the substrate. The MEMS structures were then rinsed in a hot IPA bath and dried on a hot plate at 90 °C to facilitate release.

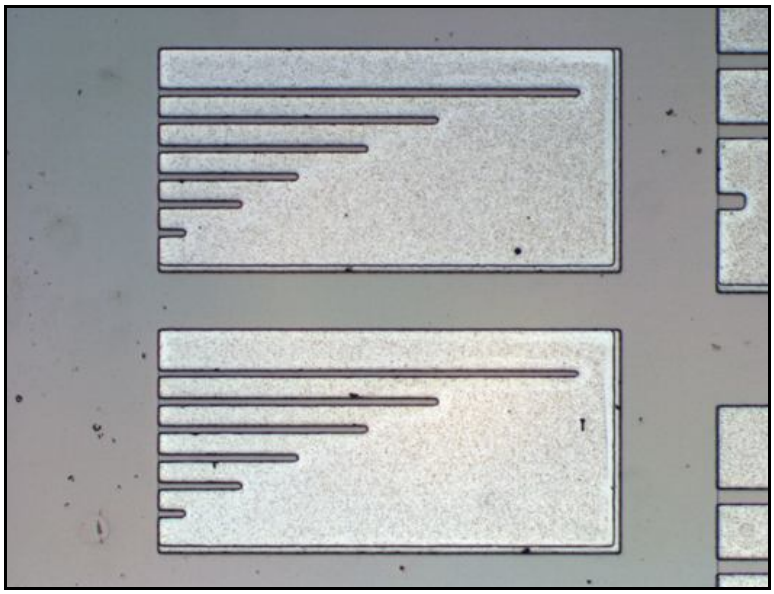


Figure 4.6 Optical image of the patterned and dry-etched poly-SiC. The lighter-colored area is the exposed sacrificial oxide. The length of the longest cantilever is 1.5mm and the width is 20μm. Note the rounded cantilever ends due to the resolution limitation of the acetate mask printing process.

4.2 Film Morphology

The surface morphology of a 20 nm and 100 nm thick polysilicon film was imaged using a PSIA XE-100 atomic force microscope (AFM) operating in tapping mode to understand how the grain size of the seed layer varies between the two depositions. Referencing Figure 4.7(a), the 20 nm thick poly-Si seed layer, and Figure 4.7(b), the 100 nm thick poly-Si seed-layer, it is clear that the grain size expands rapidly with film thickness. Maier-Schneider et al. reported an increase in the compressive strain of polysilicon films with increasing thickness. They further explain that TEM analysis of the microstructure of the film revealed that the early stages of polysilicon deposition is littered with randomly-oriented tiny grains which initially grow conically and then develop a columnar morphology. The 100 nm thick film exhibits noticeably larger,

triangular grain morphology. In fact, the grains appear to have some degree of preferred orientation.

Figures 4.7(c) and 4.7(d) are AFM scans of the poly-SiC films grown from the corresponding polysilicon seed layers shown above them. Both poly-SiC films were about 0.4 μm thick. The surface image of the poly-SiC grown on the 20 nm thick seed-layer, Figure 4.7(c), exhibits a fine, granular grain structure, whereas the poly-SiC grown on the 100 nm thick seed-layer has large, discernable polygonal-shaped grains having rounded caps and deep trenches at the boundaries. From these observations alone, one could suspect that both poly-SiC films have a stress gradient present through the thickness of the film.

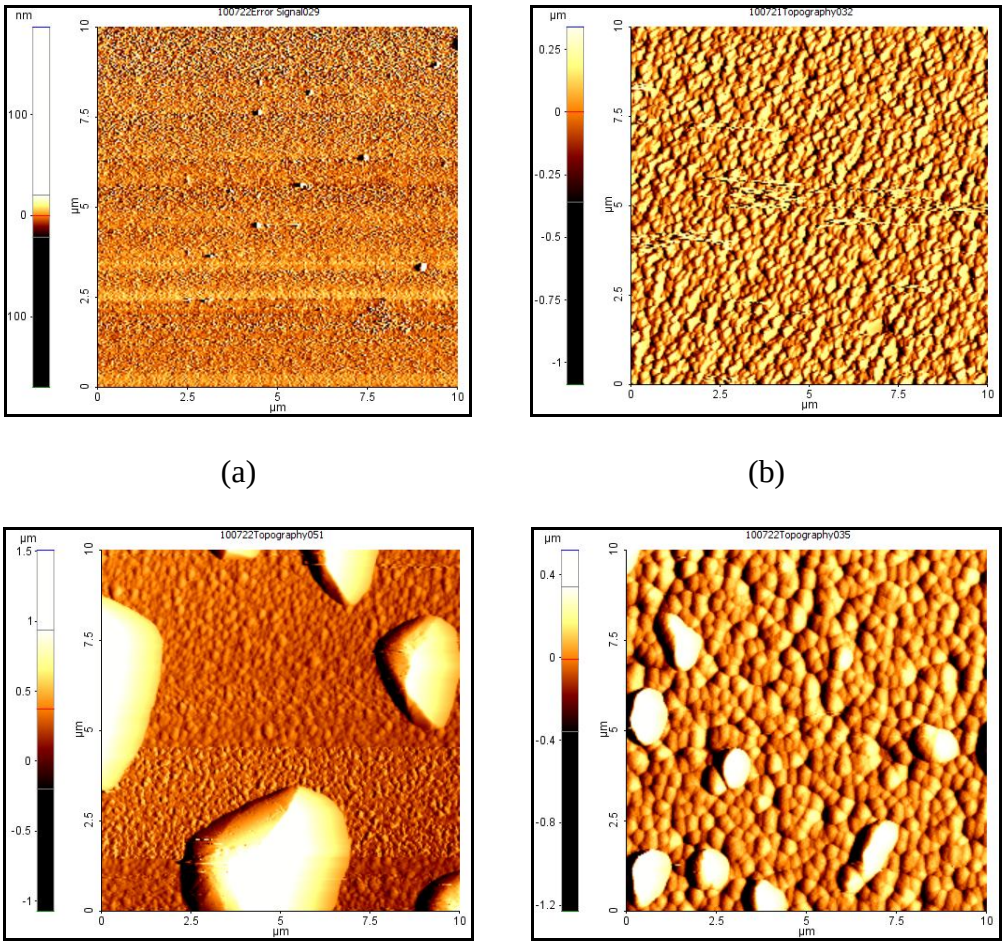


Figure 4.7 Top: Atomic force microscopy (AFM) scans of the polysilicon seed layer (a) 20nm thick and, (b) 100nm thick . Bottom: AFM scans of the corresponding poly-SiC film depositions, (c) poly-SiC film grown on the 20 nm thick polysilicon film and, (d) poly-SiC film grown on the 100 nm thick polysilicon film. Poly-SiC film thickness is ~0.5µm for both depositions. AFM data taken in tapping mode using SiN probes.

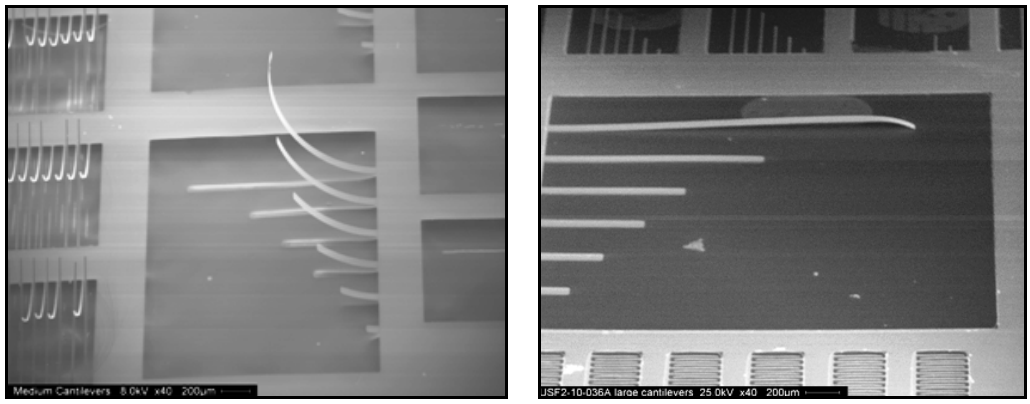
4.3 Stress-Strain Analysis

The released SiC MEMS structures were examined using a Hitachi S-800 scanning electron microscope (SEM). Comparison of the MEMS structures fabricated from the poly-3C-SiC grown on the 20 nm poly-Si seed layer and on the 100 nm poly-Si showed opposite strain gradients present in the films. As seen in Figure 4.8(a), the

polycrystalline 3C-SiC grown from the 20 nm thick seed-layer produced a large positive stress gradient which resulted in upward-bowed cantilevers. Because the poly-SiC film grown on the 100 nm polysilicon seed layer exhibited a strong negative stress gradient and the wells were shallow, meaningful measurements could not be made with the longer cantilevers since the longer cantilevers pushed into the substrate and lifted the cantilever, Figure 4.8(b). The bow present in the cantilevers fabricated from the polycrystalline 3C-SiC film grown on both substrates indicated the presence of a substantial gradient stress in both films.

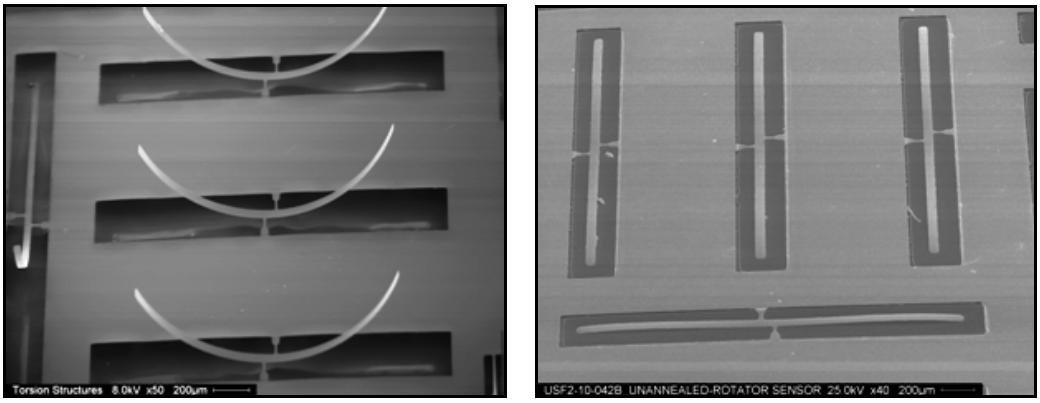
The curvature, measured far from the anchor point of the cantilevers, was assumed to be circular in the far-field and was approximated as circular segments. The chord length and segment height was measured to determine the radius of curvature, ρ, Figure 4.10(a). From these parameters, the maximum value of the stress gradient was determined using equation 2.14. The results are shown in Table 4.1.

The planar rotator structures were not sensitive enough to detect any uniform in-plane stress due to the short actuator beams not having enough length change when released from the sacrificial release layer. However, the upward curling rotators micromachined from the poly-SiC grown on the 20 nm seed-layer provided out-of-plane deformation data with minimum influence from the anchors, an issue that has to be considered for cantilever measurements near the anchor point, Figure 4.9(a). The measurements were determined in the same manner as the cantilever curvature. The results are shown in Table 4.1. Unfortunately, the large negative stress gradient of the planar rotator structures from the 100 nm seed-layer substrate pressed the beams into the substrate, Figure 4.9(b).



(a) (b)

Figure 4.8 SEM images viewed from a 45° tilt of poly-SiC cantilevers fabricated from poly-SiC grown on polysilicon-on-oxide using a (a) 20 nm thick seed layer and, (b) 100 nm thick seed layer. Note that the stress gradient is opposite in both cases indicating that the polysilicon film thickness is not yet optimized.



(a) (b)

Figure 4.9 SEM images taken at a 45° tilt angle of planar rotator structures displaying the stress gradients present in (a) poly-SiC film grown on a 20 nm polysilicon seed layer (b) poly-SiC grown on a 100 nm polysilicon seed layer.

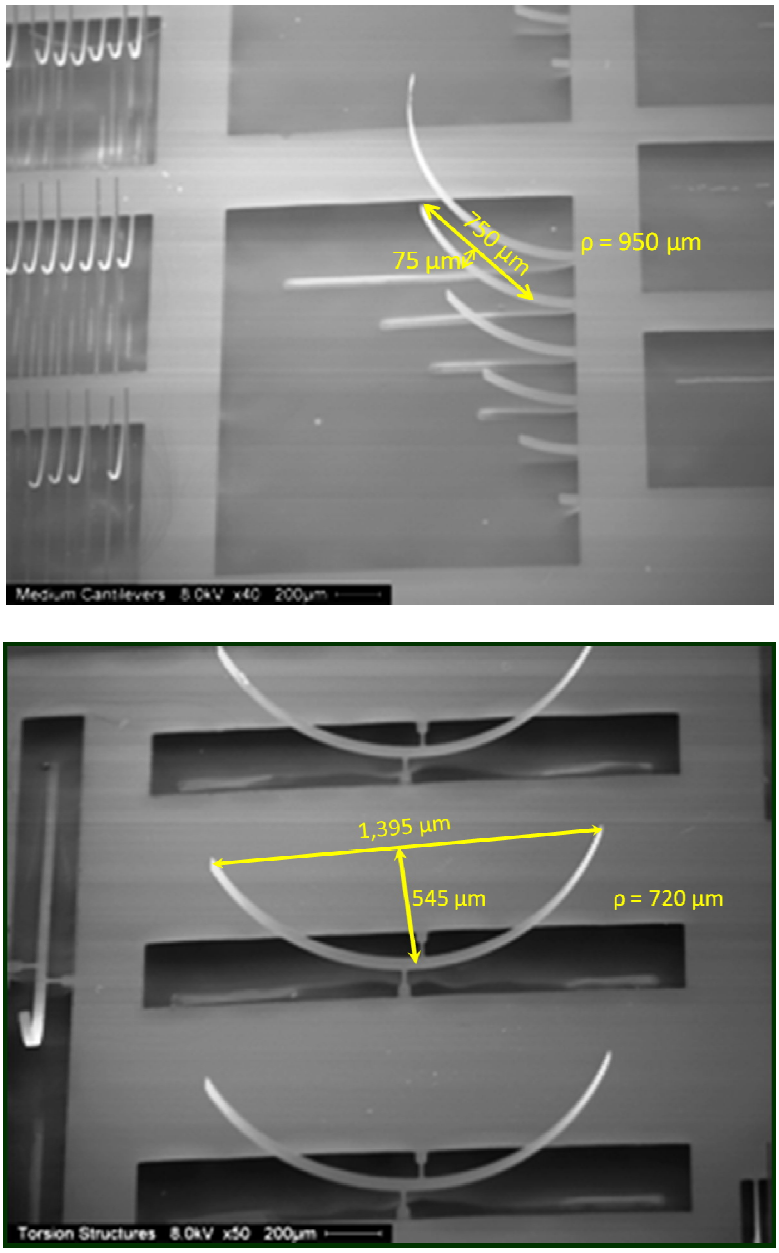


Figure 4.10 SEM image of the cantilevers from Figure 4.8(a) and the planar rotator structures from Figure 4.10(a). Dimensions corrected for the tilt projection.

Although the SEM data can provide some quantitative data for measuring the cantilever deflection, the measurements are prone to large uncertainty errors when low-angle tilt images are used. All measurements were taken using a Veeco Wyko NT9100

optical profilometer. An optical profilometer is a non-invasive method to measure the topology of a surface by using interferometry. Light is split by a beam splitter within the instrument and part of the beam passes through a microscope objective and reflects off the surface being examined. The other half of the beam serves as a reference beam and reflects off a very smooth reference mirror mounted within the optical assembly of the microscope objective. The two beams recombine and are projected on a digital camera. Depending on the length difference of the beam paths, the light will constructively or destructively interfere and form alternating light and dark fringe patterns. The focal plane of the objective lens is scanned vertically, intersecting the various surface features of the sample under investigation. The position of the servo-controlled stage is monitored with the changing light intensity of the changing fringe patterns at each pixel of the digital camera. From this information, the height information of the sample can be extracted.

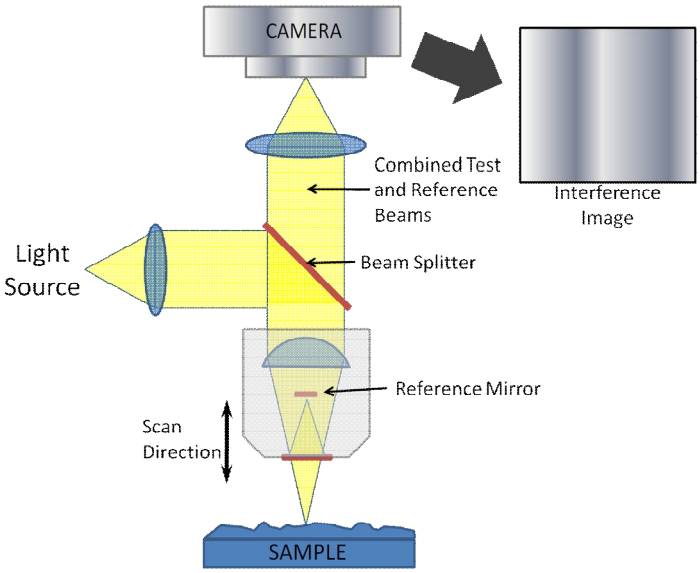
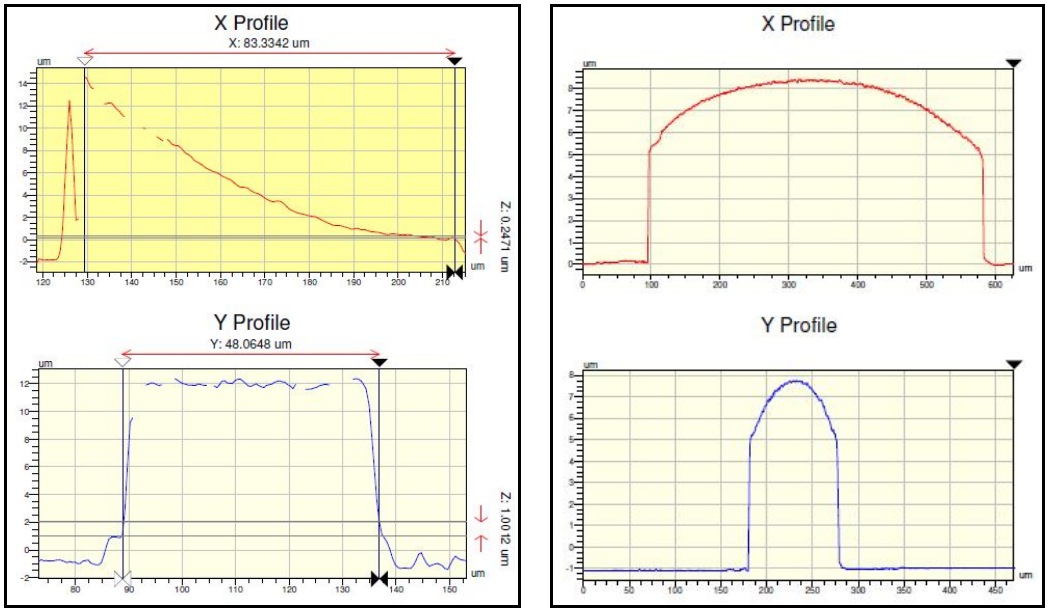


Figure 4.11 Schematic of an optical profilometer. Light is split by a beam splitter and directed through the objective to the sample surface. The reflected light is combined with a reference beam and focused on a digital camera, which records the interference image. The sample is vertically scanned and the height data is analyzed with the changing interferogram.

All measurements were made using Vertical Step Interferometry (VSI). This technique uses a white light source for reliable measurement of smooth and rough surfaces. Figure 4.10 shows topological images of the cantilevers made via optical profilometry. Optical profilometry provides quick, high-resolution surface surveys using a vertically scanning sample stage and white light interferometry. The stress gradient data obtained from the profilometry measurements are shown in Table 4.1.

Table 4.1 Maximum stress gradient values from cantilever deflection measurements acquired via optical profilometry. Positive gradient values indicate upward deflection and negative gradient values indicate downward deflection.

Structure (seed layer thick.)	Thickness (μm)	Pre-Release Length (μm)	Radius of Curvature (m)	Stress Gradient Maximum, σ_1 (MPa)
Cantilever (100 nm)	0.30	500	.0104	-41
Cantilever (100 nm)	0.30	300	.0033	-81
Planar Rotator (20 nm)	0.35	2000	7.20×10^{-6}	+130
Planar Rotator (20 nm)	0.35	2000	7.40×10^{-6}	+126
Cantilever (20 nm)	0.35	1000	9.50×10^{-6}	+101



(a) (b)

Figure 4.12 Optical profilometer data of poly-SiC cantilevers micromachined from poly-SiC grown from (a) a 20 nm poly-Si seed layer and, (b) a 100 nm thick poly-Si seed layer. Notice that bowing is present in the X profile and Y profile data due to biaxial bending. Also note the scale difference between both profiles exaggerates the bowing in the Y profile. Images courtesy of Richard Everly, USF-NREC, Tampa FL.

CHAPTER 5: SUMMARY AND FUTURE WORKS

5.1 Summary

A low temperature heteroepitaxial process has been developed and characterized for the growth of 3C-SiC on 50 mm (111)Si substrates. A "baseline" high temperature process was first developed from a previously established 3C-SiC on (100)Si high temperature growth process. From this baseline process, a low temperature baseline process at 1200°C was developed, optimized and then applied to 3C-SiC growth on a poly-Si/ SiO_2/ (111)Si compliant substrate stack.

The initial base line for 3C-SiC deposition was achieved using a two-step growth process, carbonization of the Si substrates proceeded with a growth plateau. The substrate was first heated from room temperature to 1135°C in a mixture of a H_2/C_3H_8 (10 slm/16 sccm) at 400 Torr. Once at 1135°C, the substrate was maintained at this temperature for two minutes to carbonize the surface. The temperature was then increased from 1135°C to 1380°C. During this temperature ramp, the H_2 flow was increased to 40 slm and the pressure was reduced from 400 Torr to 100 Torr. The SiH_4 was introduced into the gas mixture at 10sccm and increased at intervals to the final flow rate of 220sccm. Meanwhile, the propane was simultaneously decreased at intervals to 6 sccm. The resulting film was specular and demonstrated low crystal defects as measured via XRD and TEM analysis.

The high temperature baseline process was then adapted for low temperature growth. The carbonization occurred at 1135°C while 10 slm of H_2 and 16 sccm of C_3H_8 flowed through the reactor. The carbonization process lasted for a two minute duration. The temperature was ramped from 1135°C to 1200°C. It was discovered after several low temperature optimization experiments that a lower flow rate of the H_2 carrier was required than the high temperature growth process. During the temperature ramp from the carbonization plateau to the growth plateau, a H_2 flow rate of 25 slm was implemented. In order to increase the deposition rate at the lower temperature, the growth pressure was decreased to 75 Torr, the minimum chamber pressure possible for the MF2 CVD reactor. Under these optimized conditions, the deposition rate improved from 1.4 μm/h to 1.9 μm/h with the transparent film exhibiting a smooth, specular morphology.

Finally, the optimized low temperature process was used to deposit 3C-SiC on an oxide compliant substrate. Compliant substrates should soften at the deposition temperature and allow the strain inherent to heteroepitaxy to reside in the substrate thus ensuring a high-quality film is formed. Deposition experiments on the poly-Si/ SiO_2/ (111)Si stacks and various orientations of crystalline Si substrates were performed in tandem. Initial measurements using XRD revealed crystal quality that rivaled or exceeded the films deposited on the crystalline Si substrates. Further investigation using TEM and AFM analysis revealed that the films deposited on the compliant substrate stack were highly-textured polycrystalline silicon carbide which seems to be ideal for MEMS applications.

Based on this result MEMS structures were designed and structures fabricated in order to fully determine the stress-strain relationship in these poly-SiC on polysilicon films. Successful MEMS structures, consisting of cantilevers, bridges, comb drives and rotating probes, were realized in two sets of experiments. In the first set an acetate mask was used to allow rapid prototyping of the MEMS process (resolution 20 μm). These results helped to define the optimum polysilicon deposition thickness and temperature, and it was shown that poly-SiC structures fabricated on 20 nm and 100 nm thick polysilicon films contained tensile and compressive residual stress (i.e., cantilevers were bowed up and down, respectively). Based on these important findings, a more accurate mask set was designed and fabricated using chrome on quartz.

5.2 Future Work

A cost-effective growth process capable of producing low stress SiC will need to be developed in order for silicon carbide to be considered a commercially viable material for electronic and MEMS applications. Unfortunately, (111) oriented 3C-SiC films grown directly on crystalline Si substrates are plagued by stress-related issues, such as film deformation, commonly referred to as wafer bow, and fracturing, that overwhelm any benefits achieved to date. Several techniques have been investigated to overcome the mismatch issues associated with SiC heteroepitaxial growth, but compliant substrates offer the most promising approach for the realization of devices formed on mismatched heteroepitaxial materials (Ayers 2008). A wide variety of compliance methods have been developed over the years where a majority of the methods involve a thin film serving as a crystal seed template layer for epitaxial growth that decouples the thicker substrate from

the epitaxial film (Ayers 2008). The benefit of using an oxide-based compliant substrate is that the oxide can be easily etched away thus it serves double duty as a MEMS release layer. This would be invaluable for the advancement of the SiC-based MEMS and bio-MEMS which is the research vision of the USF SiC Group at the University of South Florida.

5.2.1 3C-SiC Growth on SOI Substrates

As previously discussed, oxide-based compliant substrates offer a stress-relaxation mechanism and the benefit of an etch-stop release layer. The work done on the poly-Si/ SiO_2/ Si compliance stack offers many avenues to explore. While the benefit of using a CVD deposited poly-seed layer is that it can be deposited using readily accessible tools, producing the very thin films necessary for compliancy, but potentially leaving "pinholes" within the seed-layer. A viable solution to overcome this issue is to grow thicker CVD deposited Si films and follow with dry oxidation and HF etching of the Si layer. The low oxidation rate of dry oxidation would offer better control of the seed layer thickness. The poly-Si/ SiO_2/ Si stack produces highly-oriented polycrystalline 3C-SiC, but a monocrystalline template is needed to produce highly crystalline 3C-SiC. Initial work in the USF SiC Group involved the growth of 3C-SiC on SOI via cold-wall CVD. This work was conducted by Dr. R. L. Myers-Ward during her MS thesis research using silicon bonded wafers produced by Dr. Karl Hobart of NRL. Work on this Si/ poly-SiC SOI substrate was continued by S. Harvey via hot-wall CVD using the MF1 reactor (Harvey 2006).

The compliancy of the oxide layer could be supplemented with the incorporation of various dopants into the silicon over layer (SOL) of the SOI substrate to create a buffer layer to deposit 3C-SiC. $Si_xGe_{(1-x)}$ alloys have already been incorporated into the SOL of SOI substrates and have demonstrated improved epitaxial film quality when compared to non-compliant substrates (Ayers 2008). What was lacking during the previous work on SOI substrates in our group was a high-quality, low-temperature 3C-SiC on Si growth process and now that this process has been developed as part of this work perhaps it is time to revisit SOI as a means to form high-quality films for electronic device applications.

5.2.2 Residual Stress Characterization

The fundamental issue regarding heteroepitaxial growth, or any film growth for that matter, is the degree of in-plane film stress and how the film responds to that stress. Characterization the 3C-SiC film stress is going to be necessary in order to quantify and evaluate the effectiveness of 3C-SiC growth on future compliant substrates. Only recently have tools become readily available at USF to make the necessary measurements. A recently established collaboration with Dr. A. Volinsky in the mechanical engineering department has provided us with new characterization opportunities. Nanoindentation can provide important data regarding film hardness and fracture toughness. Several tools are available for wafer/film deformation analysis from which film stress can be extracted via the modified Stoney's equation. While deformation analysis provides valuable stress-related data, it tends to be sensitive and assumptions made in the derivation of the modified Stoney's equation can produce large

errors. Other techniques will need to be incorporated in order to supplement this data. Micro Raman Spectroscopy and XRD analysis can prove useful for quantifying in-plane film strain/ stress of highly-textured 3C-SiC films by measuring the peak-shifts in stressed films, however XRD can be very sensitive to measurement error if the peaks are located at $2\theta < 90°$. Incorporation of these stress analysis techniques into the current characterization protocol of the SiC Group at USF will provide enhanced feedback for continued improvement of the 3C-SiC heteroepitaxy process.

5.2.3 MEMS Fabrication

Perhaps the most obvious future work task emanating from this thesis research is to take the materials developed and form high-quality MEMS structures, either for mechanical MEMS or bio-MEMS applications. Given the thrust of the USF SiC group into the bioengineering arena, this work would support a whole host of research on-going in the group and thus allow for critical mass to be achieved, which is difficult to do in a university research group that is not located within a research center. Three tasks are recommended in this area.

1) micro-machine 3C-SiC on (100)Si films and compare stress values to realized structure bow so as to correlate and correct stress measurement analysis and modified Stoney's equation methods discussed in the previous section.

2) grow additional poly-3C-SiC on oxide films, micro-machine them and compare the structure bow with pre-release mechanical stress measurements to see how well they correlate. And, finally

3) re-start 3C-SiC on SOI substrate research, both for MEMS applications as well as realizing high-quality 3C-SiC films for electronic applications.

If these 3 tasks are pursued there is a high probability that breakthroughs in 3C-SiC on Si technology can be made so that this polytype of SiC, the so called ‘dark horse’ of SiC, can take its place as the preferred polytype due to its lower cost of epi growth and possibility for realization on large-area, inexpensive Si substrates. To achieve this goal clearly more work needs to be done but the ground work has been laid in this thesis research as well as others around the world and there is hope that this dream may become a reality in the near future.

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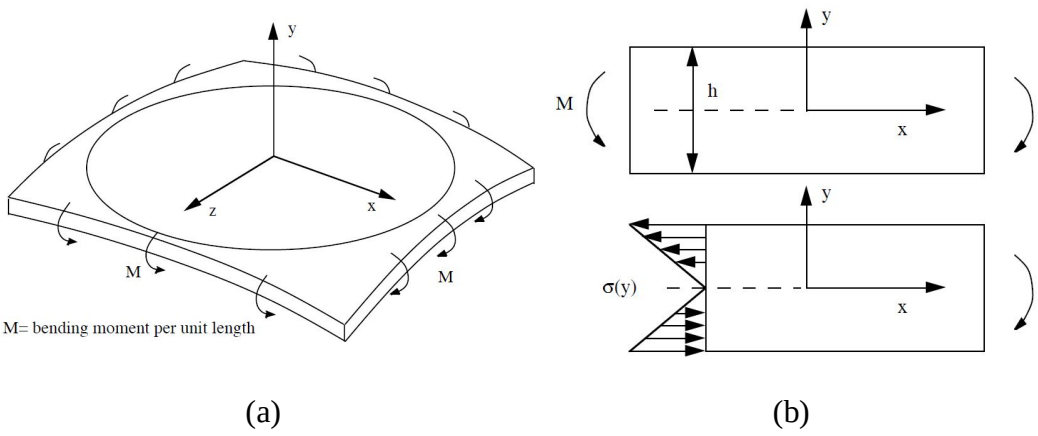
APPENDICES

Appendix A Mechanics of the Biaxial Deflection of a Plate

Many of the results used to analyze the mechanical properties of thin films are based on the solutions to fundamental mechanical problems, e.g. a simply bent beam, a plate deformed by a bending moment, etc. When a film has a thickness, t_f, that is substantially smaller than the lateral length, L, and thickness of the substrate on which the film is deposited, t_s, then simple beam mechanics can be applied to understand the deflection response of the film to an applied force. The stress state of the film-substrate system is analyzed using the biaxial deflection of a plate as a model, shown in Figure 2.14(a).



(a) (b)

Figure A.1 (a) Schematic of a bending moment applied to a plate and a cross-section diagram (b) showing the resulting stress gradient.

Referring to Figure 2.14(b), a beam has a bending moment, M, applied so the beam is placed in a pure bending state. The origin of the coordinate system is located at

the neutral axis of the purely bent beam. The isotropic, biaxial stress distribution directed along the length of the simple bent beam is given by:

$$\sigma_{xx} = \sigma_{zz} = \alpha \cdot y \tag{2.6}$$

The first subscript denotes the direction of the applied force (stress) and the second subscript denotes the direction of the normal of the plane on which the force (stress) is being applied. For example, σ_{xx} means the force (stress) is directed along the x-axis and is applied to the plane whose normal is parallel to the x-axis, in the case of Figure 2.14(b), the y-z plane. The distance from the neutral axis along the y-direction, y, is the moment arm.

By relating the bending stresses in the beam with the bending moment, α can be found:

$$M = \int_{-h/2}^{+h/2} \sigma_{xx} \cdot y dy = \int_{-h/2}^{+h/2} \alpha \cdot y^2 dy = \frac{\alpha \cdot h^3}{12} \tag{2.7}$$

$$\alpha = \frac{12 \cdot M}{h^3}$$

Inserting into equation 2.6 yields,

$$\sigma_{xx} = \sigma_{zz} = \frac{12 \cdot M \cdot y}{h^3} \tag{2.8}$$

Referencing Figure 2.15, an expression is derived relating the bending strain of a beam to the curvature. Using equation 2.3 and the relationship of the arc length to the subtended angle and radius (i.e. definition of a radian), the following expression is defined:

$$\varepsilon_{xx}(y) = \frac{\Delta L}{L} = \frac{((R+y)\cdot\theta - R\cdot\theta)}{R\cdot\theta} = \frac{y}{R} = -\kappa \cdot y \tag{2.9}$$

Where, κ, is the curvature of the beam. Rearranging equation 2.9 yields the relationship between curvature and the strain in the beam.

$$\kappa = -\frac{1}{R} = \frac{-\varepsilon_{xx}(y)}{y} \tag{2.10}$$

Appendix A (Continued)

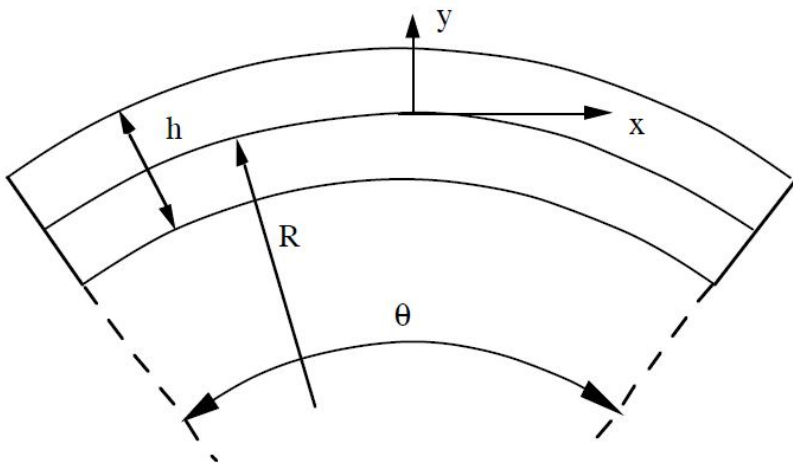


Figure A.2 Geometric parameters defining a simply bent beam.

In order to calculate the strain, $\varepsilon_{xx}(y)$, from the strain-curvature relationship of equation 2.10, we employ Hooke's Law:

$$\varepsilon_{xx} = \left(\frac{1}{E}\right)\cdot\left(\sigma_{xx} - \nu\left(\sigma_{yy} + \sigma_{zz}\right)\right) \tag{2.11}$$

Since the biaxial stress is isotropic in the plane of the film ($\sigma_{xx} = \sigma_{zz}$), no stress fields exist in the y-direction ($\sigma_{yy} = 0$), and the magnitudes of the bending stress-strain are dependent on the y-distance from the neutral axis, equation 2.11 reduces to:

$$\varepsilon_{xx}(y) = \left(\frac{1-\nu}{E}\right)\cdot\sigma_{xx}(y) \tag{2.12}$$

Appendix A (Continued)

Replacing $\sigma_{xx}(y)$ with the result from the moment analysis in which the stress was related to the bending moment (equation 2.8), and then incorporating the relationship between curvature and strain (equation 2.10), the relation between curvature and the applied moment is:

$$\kappa = -\left(\frac{(1-\nu)}{E}\right)\cdot\left(\frac{12\cdot M}{h^3}\right) \tag{2.13}$$

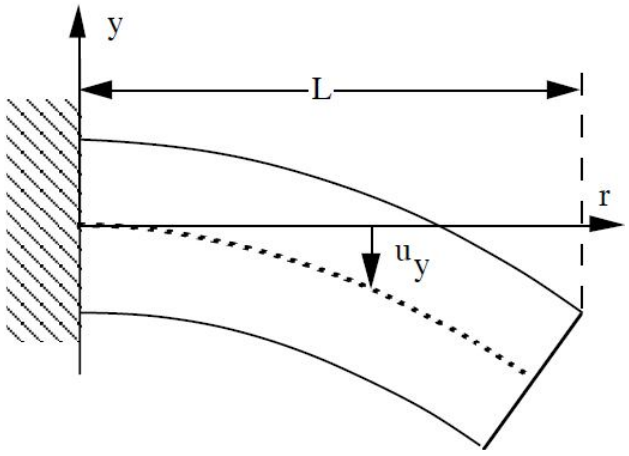


Figure A.3 Cantilever deformed by a bending moment.